

Edoardo Charbon

Citizenship: Switzerland

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Education:

1995 – Ph.D., University of California at Berkeley – Major: EECS

1991 – M.S., University of California at San Diego – Major: ECE

1988 – El. Ing. Diploma, ETH-Zürich – Abteilung: Elektrotechnik

Areas of Expertise:

2D/3D Optical Imager Design

Electronic intellectual property protection tools and flows

CAD tools for radio-frequency analog and mixed-signal circuits

Optimization techniques: theory and implementation

Numerical substrate/temperature analysis and circuit simulation

Ultra low-noise IC design for instrumentation and sensor applications

Professional Experience:

2002 – Present

Professor – Dept. of ECE (I&C)

EPFL, Lausanne, Switzerland

2000 – 2002

Chief Architect

Canesta Inc., San Jose, California

2D/3D Imaging systems

1995 – 2002

Post-doctoral fellow – ERL

University of California at Berkeley

Substrate extraction and optimization via Discrete Fourier Transform

Reduced noise models for high-speed digital blocks substrate injectors

First published intellectual property protection scheme for FSMs and hierarchical designs

1995 – 2000

Senior member of technical staff / architect – Custom IC Group / iDesign

Cadence Design Systems, Inc., San Jose, California

Physical Design Constraint Manager

Company-wide intellectual property protection initiative

1991 – 1995

Graduate student/Research assistant – CAD group

University of California at Berkeley

Constraint-based physical design CAD for deep submicron ICs

Design and fabrication of a D/A converters and a phase lock loops

- First published router for microwave ICs
Advanced models for inductive components in Superconductive ICs
- 1993
R&D Engineer – System Division
Hewlett-Packard (Agilent) Santa Rosa, California
Performance-driven layout tools for RF and microwave circuits
- 1991
R&D Engineer – TCAD Research
Texas Instruments, Dallas, Texas
Reliability-driven tools for mixed-mode applications
- 1990
Visiting researcher – Dept. of EE
University of Waterloo, Canada
Fabrication and test of ultra low-noise, nano-Tesla magnetic sensor ICs
- 1989 – 1991
Graduate student – Dept. of ECE (Telecommunications Division)
University of California at San Diego
Analytical models for concurrent queueing systems
Scalable concurrent communication protocols
- 1986
R&D Intern – Switched Capacitor Dept.
ITALTEL SpA., Milano, Italy
High-precision analog ICs for Switched Capacitor applications

Honors and Awards:

- Best Paper Award Nominee, Custom Integrated Circuits Conference, 1999
Cadence Quality Award, San Jose, California, 1997
Special Achievement Award, San Jose, California, 1997
National Science Foundation Fellowship Award, Switzerland, 1991
Asea Brown Boveri Advanced Research Award, Switzerland, 1989 and 1992
The Lehmann Foundation Special Award, Switzerland, 1989

Reviewer:

- Journal of Solid-State Circuits, Trans. on Circuits and Systems, Trans. IWSM, Trans. on Computer Aided Design, Trans. on VLSI, Integration, Custom Integrated Circuits Conference, Design Automation Conference, International Conference on Computer Aided Design, Sensors & Actuators

Miscellaneous:

- Guest Editor, Journal of Solid-State Circuits, 2002–
CICC Technical Committee member, 1999–
Guest Editor, Trans. on CAD, 1999
UC-Berkeley Student Admission Committee member, 1995
IEEE member, 1989–
Swiss Scientist Association, America
Swiss National Radio reports from the Silicon Valley, 1997-1998

Refereed Journal Articles, Editorials, Books:

- [1] H. Baltès, E. Charbon, M. Parameswaran, and A. Robinson
Humidity-sensitive Oscillator Fabricated in Double Poly CMOS Technology,
Sensors and Actuators B (Chemical), Vol. B 1, N. 1-6, pp. 441-445, Jan 1990
- [2] A. Nathan, E. Charbon, W. Kung and A. Salim,
Low-Frequency Noise Correlations in Lateral PNP Bipolar Transistors,
Canadian Journal of Physics, Vol.70, N. 10-11, pp. 1112-17, Oct.-Nov. 1992
- [3] P. Xiao, E. Charbon, A. Sangiovanni-Vincentelli, T. van Duzer and S. Whiteley,
INDEX: An Inductance Extractor for Superconducting Circuits,
IEEE Trans. on Applied Superconductivity, Vol.3, N. 1, pt.4, pp. 2629-32, March 1993
- [4] E. Malavasi, H. Chang, A. Sangiovanni-Vincentelli, E. Charbon, U. Choudhury, G. Jusuf, E. Liu, and R. Neff,
A Top-down, Constraint-Driven Design Methodology for Analog Integrated Circuits,
In Ed. Book. Analog Circuit Design, pp. 285-324, Kluwer Academic Publishers, Dordrecht, The Netherlands, 1993
- [5] E. Malavasi, E. Felt, E. Charbon, A. Sangiovanni-Vincentelli,
Performance-Driven Compaction of Analog IC's,
In International Journal of Circuit Theory and Applications, Special Issue on Analog Tools for Circuit Design, pp. 433-452, John Wiley & Sons, July-August 1995
- [6] E. Malavasi, E. Charbon, E. Felt, A. Sangiovanni-Vincentelli,
Automation of IC Layout with Analog Constraints,
In IEEE Trans. on Computer Aided Design, Vol. CAD-15, N. 8, pp. 923-942, August 1996
- [7] H. Chang, E. Charbon, U. Choudhury, A. Demir, E. Felt, E. Liu, E. Malavasi, A. Sangiovanni-Vincentelli, and I. Vassiliou,
A Top-Down, Constraint-Driven Design Methodology for Analog ICs,
Kluwer Academics Publishers, 1996
- [8] E. Charbon, E. Malavasi, P. Miliozzi, A. Sangiovanni-Vincentelli,
Non-Deterministic Constraint Generation for Analog and Mixed-Signal Layout,
In IEICE Trans. on Inf. & Syst., Vol. E80-D, N. 10, pp. 1032-1043, October 1997
- [9] E. Charbon, R. Gharpurey, R. G. Meyer, and A. Sangiovanni-Vincentelli,
Substrate Optimization Based on Semi-Analytical Techniques,
In IEEE Trans. on Computer Aided Design, Vol. CAD-18, N. 2, pp. 172-190, February 1999
- [10] E. Charbon, P. Miliozzi, L. Carloni, A. Ferrari, and A. Sangiovanni-Vincentelli,
Modeling Digital Substrate Noise Injection in Mixed-Signal ICs,
In IEEE Trans. on Computer Aided Design, Vol. CAD-18, N. 3, pp. 301-310, March 1999
- [11] E. Malavasi and E. Charbon,
Constraint Transformation for IC Physical Design,
In IEEE Trans. on Semiconductor Manufacturing, Vol. 12, N. 4, pp. 386-395, November 1999
- [12] | I. Torunoglu and E. Charbon,

Watermarking-Based Copyright Protection of Sequential Functions,
In IEEE Journal of Solid-State Circuits, Vol. 35, N. 3, pp. 434-440, March 2000

[13] E. Charbon and R. Saleh,
Guest Editorial,
In IEEE Trans. on Computer Aided Design, Vol. CAD-19, N. 6, June 2000

[14] E. Charbon, R. Gharpurey, P. Miliozzi, R.G. Meyer, and A. Sangiovanni-Vincentelli,
Substrate Noise: Analysis and Optimization for IC Design,
Kluwer Academics Publishers, March 2001

[15] P. Miliozzi, L. Carloni, E. Charbon, A. Sangiovanni-Vincentelli,
SubWave: a Methodology for Modeling Digital Substrate Noise Injection in Mixed-Signal ICs,
In Ed. Book, Signal Integrity Effects in Custom IC and ASIC Designs, IEEE, November 2001

[16] E. Charbon and I. Torunoglu,
Watermarking Techniques for Electronic Circuit Design,
In Lecture Notes on Computer Science, Springer Verlag, Vol. 2613, pp. 147-169, May 2003

[17] F. Svelto, E. Charbon, and S. Wilton
Guest Editorial,
In IEEE Journal of Solid-State Circuits, Vol. SC-38, N. 3, March 2003

Refereed and Invited Proceedings Articles:

[18] E. Malavasi, E. Charbon, G. Jusuf, R. Totaro and A. Sangiovanni-Vincentelli,
Virtual Symmetry Axes for the Layout of Analog ICs,
In Proc. ICVC, pages 195-198, Seoul, Korea, October 1991

[19] E. Charbon, E. Malavasi, U. Choudhury, A. Casotto and A. Sangiovanni-Vincentelli,
A Constraint-Driven Placement Methodology for Analog Integrated Circuits,
In Proc. IEEE Custom Integrated Circuits Conference, pp. 2821-2824, Boston, May 1992

[20] H. Chang, A. Sangiovanni-Vincentelli, F. Balarin, E. Charbon, U. Choudhury, G. Jusuf, E. Liu, E. Malavasi, R. Neff and P. Gray,
A Top-down, Constraint-Driven Design Methodology for Analog Integrated Circuits,
In Proc. IEEE Custom Integrated Circuit Conference, pp. 841-846, Boston, May 1992

[21] E. Felt, E. Charbon, E. Malavasi and A. Sangiovanni-Vincentelli,
An Efficient Methodology for Symbolic Compaction of Analog IC's with Multiple Symmetry Constraints,
In Proc. EuroDAC, pages 148-153, Hamburg, Germany, September 1992

[22] E. Felt, E. Malavasi, E. Charbon and A. Sangiovanni-Vincentelli,
Performance-Driven Compaction for Analog Integrated Circuits,
In Proc. IEEE Custom Integrated Circuit Conference, pp. 1731-1735, San Diego, May 1993

- [23] E. Charbon, E. Malavasi and A. Sangiovanni-Vincentelli, Generalized Constraint Generation for Analog Circuit Design, In Proc. IEEE International Conference on Computer Aided Design, pp. 408-414, Santa Clara, November 1993
- [24] E. Charbon, E. Malavasi, D. Pandini and A. Sangiovanni-Vincentelli, Imposing Tight Specifications on Analog IC's through Simultaneous Placement and Module Optimization, In Proc. IEEE Custom Integrated Circuit Conference, pp. 525-528, San Diego, May 1994
- [25] H. Chang, E. Liu, R. Neff, E. Felt, E. Malavasi, E. Charbon, A. Sangiovanni-Vincentelli and P. R. Gray, Top-Down, Constraint-Driven Methodology Based Generation of n-bit Interpolative Current Source D/A Converters, In Proc. IEEE Custom Integrated Circuit Conference, pp. 369-372, San Diego, May 1994
- [26] E. Charbon, E. Malavasi, D. Pandini, A. Sangiovanni-Vincentelli, Simultaneous Placement and Module Optimization of Analog IC's, In Proc. IEEE Design Automation Conference, pp. 31-35, San Diego, June 1994
- [27] E. Charbon, G. Holmlund, B. Donecker, A. Sangiovanni-Vincentelli, A Performance-Driven Router for RF and Microwave Analog Circuit Design, in Proc. IEEE Custom Integrated Circuit Conference, pp. 383-386, Santa Clara, May 1995
- [28] P. Miliozzi, L. Carloni, E. Charbon, A. Sangiovanni-Vincentelli, SubWave: a Methodology for Modeling Digital Substrate Noise Injection in Mixed-Signal ICs, in Proc. IEEE Custom Integrated Circuit Conference, pp. 385-388, San Diego, May 1996
- [29] P. Miliozzi, I. Vassiliou, E. Charbon, E. Malavasi, A. Sangiovanni-Vincentelli, Use of Sensitivities and Generalized Substrate Models in Mixed-Signal IC Design, in Proc. IEEE Design Automation Conference, pp. 227-232, Las Vegas, June 1996.
- [30] E. Charbon, P. Miliozzi, E. Malavasi, A. Sangiovanni-Vincentelli, Generalized Constraint Generation in the Presence of Non-Deterministic Parasitics, In Proc. IEEE International Conference on Computer Aided Design, pp. 187-192, San Jose, November 1996
- [31] E. Charbon, R. Gharpurey, R. G. Meyer, A. Sangiovanni-Vincentelli, Semi-Analytical Techniques for Substrate Characterization in the Design of Mixed-Signal ICs, In Proc. IEEE International Conference on Computer Aided Design, pp. 455-462, San Jose, November 1996
- [32] I. Vassiliou, H. Chang, A. Demir, E. Charbon, P. Miliozzi, A. Sangiovanni-Vincentelli, A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology, In Proc. IEEE International Conference on Computer Aided Design, pp. 463-468, San Jose, November 1996

- [33] E. Charbon, E. Malavasi, P. Miliozzi, A. Sangiovanni-Vincentelli,
Generation and Handling of Non-Deterministic Parasitic Constraints in Analog and Mixed-Signal IC Layout Synthesis,
In Proc. Sixth Workshop on Synthesis And System Integration of MIXed Technologies, pp. 221-227, Fukuoka, Japan, November 1996.
- [34] E. Malavasi, J. Ganley, E. Charbon,
Quick Placement with Geometric Constraints,
In Proc. IEEE Custom Integrated Circuit Conference, pp. 561-564, San Diego, May 1997
- [35] E. Charbon,
Hierarchical Watermarking in IC Design,
In Proc. IEEE Custom Integrated Circuit Conference, pp. 295-298, Santa Clara, May 1998
- [36] B.G. Arsintescu, E. Charbon, E. Malavasi,
AC Constraint Transformation for Top-Down Analog Design,
In Proc. IEEE International Symposium on Circuits and Systems, Monterey, pp. 126-30, Vol. 6, June 1998
- [37] B.G. Arsintescu, E. Charbon, E. Malavasi, U. Choudhury, W. Kao,
General AC Constraint Transformation for Analog ICs,
In Proc. IEEE Design Automation Conference, pp. 38-43, San Francisco, June 1998
- [38] E. Malavasi and E. Charbon,
Constraint Transformation for IC Physical Design,
In Proc. IEEE Workshop on Statistical Metrology, Hawaii, pp. 46-49, June 1998
- [39] E. Malavasi, E. Charbon, B.G. Arsintescu, W. Kao,
A Constraint Management System for IC Physical Design,
In Proc. XI Brazilian Symposium on Integrated Circuit Design, pp. 240-243, Rio de Janeiro, October 1998
- [40] E. Charbon and I. Torunoglu,
Intellectual Property Protection Via Hierarchical Watermarking,
In Proc. International Workshop On IP Based Synthesis and System Design, Grenoble, December 1998
- [41] E. Charbon and I. Torunoglu,
Watermarking Layout Topologies,
In Proc. Asia-South Pacific Design Automation Conference, pp. 213-216, Hong Kong, January 1999
- [42] I. Torunoglu and E. Charbon,
Watermarking-Based Copyright Protection of Sequential Functions,
In Proc. IEEE Custom Integrated Circuit Conference, pp. 35-38, San Diego, May 1999
- [43] E. Charbon and I. Torunoglu,
Copyright Protection of Designs Based on Multi Source IPs,
In Proc. IEEE International Conference on Computer Aided Design, pp. 591-595, November 1999

- [44] E. Charbon and J. Phillips,
Substrate Noise: Analysis, Models, and Optimization (INVITED)
In Proc. VLSI, pp. 456-472, Lisbon, December 1999
- [45] E. Charbon and I. Torunoglu,
Digital Fingerprinting of Virtual Components,
In Proc. International Workshop On IP Based Synthesis and System Design, pp. 221-224,
Grenoble, December 1999
- [46] E. Charbon, L. M. Silveira, P. Miliozzi,
A Benchmark Suite for Substrate Analysis,
In Proc. Asia South-Pacific Design Automation Conference, pp. 617-621, Tokyo, January 2000
- [47] E. Charbon and I. Torunoglu,
On Intellectual Property Protection (INVITED),
In Proc. IEEE Custom Integrated Circuits Conference, pp. 517-523, Orlando, May 2000
- [48] S. Zanella, A. Neviani, E. Zanoni, P. Miliozzi, E. Charbon, C. Guardiani, L. Carloni, and
A. Sangiovanni-Vincentelli,
Modeling of Substrate Noise Injected by Digital IP Libraries,
In Proc. IEEE International Symposium on Quality Electronic Design, pp. 488-492, San Jose,
March 2001
- [49] E. Charbon and I. Torunoglu,
Watermarking Techniques for Electronic Circuit Design,
In Proc. International Workshop on Digital Watermarking, pp. 173-195, November 2002
- [50] C. Niclass, A. Rochas, P.A. Besse, and E. Charbon,
A CMOS Single Photon Avalanche Diode Array for 3D Imaging,
to appear in Proc. IEEE International Solid-State Circuits Conference, February 2004

Patents:

U.S. 6,515,740 - **Methods for CMOS-compatible three-dimensional image sensing using quantum efficiency modulation**
February 4, 2003

U.S. 6,522,395 - **Noise reduction techniques for three-dimensional information acquirable with CMOS-compatible sensor ICs**
February 18, 2003

U.S. 6,580,496 - **Systems for CMOS-compatible three-dimensional image sensing using quantum efficiency modulation**
June 17, 2003

U.S. 6,587,186 - **CMOS-compatible three-dimensional image sensing using reduced peak energy**
July 1, 2003

U.S. 6,625,780 - **Watermarking based protection of virtual component blocks**
September 23, 2003