EECS 290Y FALL 1993

PROJECT PRESENTATION

A 12b 500kHZ SECOND ORDER SIGMA DELTA A/D CONVERTER

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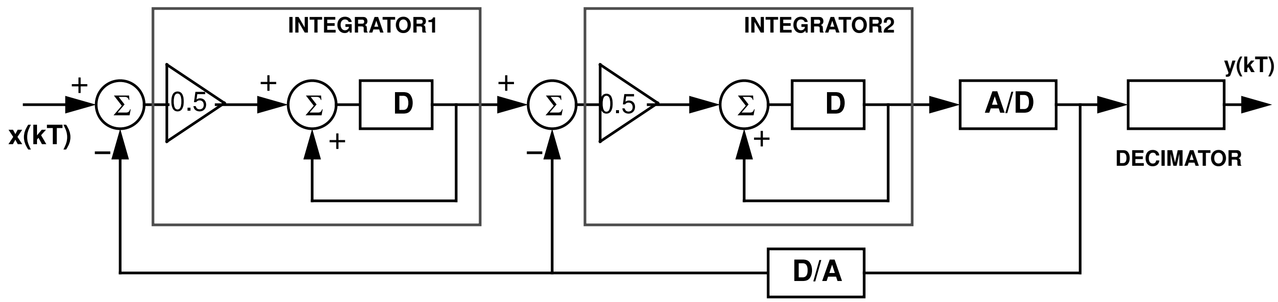
OUTLINE OF PRESENTATION

- MODULATOR ARCHITECTURE SELECTION
- METHODOLOGY
- HIGH LEVEL CONSTRAINTS GENERATION
- IMPLEMENTATION
- SIMULATION RESULTS
- CONCLUSION

MODIFIED SECOND ORDER ΣΔ MODULATOR



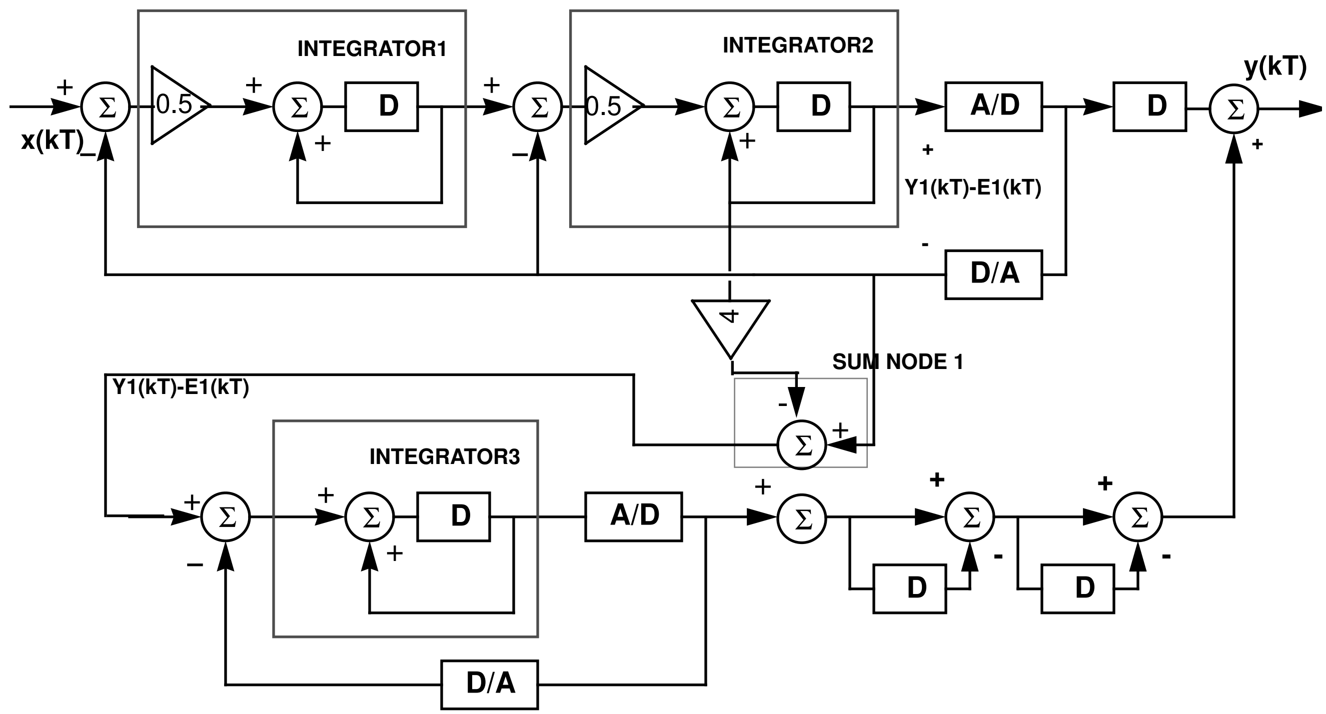
ADVANTAGES

- Robust and stable with proper amplitude scaling
- Low Complexity

DISADVANTAGES

- Tight constraints on building blocks for high resolution

THIRD ORDER CASCADE 2+1 ΣΔ MODULATOR



THIRD ORDER CASCADE 2+1 ΣΔ MODULATOR

ADVANTAGES

- Third order noise shaping increases SNR for same M
- Cascade of 2 stable modulators - robust
- Lower constraints on circuit blocks - integrator, comparator

DISADVANTAGES

- Increased complexity
- Circuit sensitive to gain mismatch - may get second order noise shaping error
- More difficult optimization of parameters - gain factors, etc

WHICH MODULATOR ?

SECOND ORDER ΣΔ

- Relatively low SNR requirement
- Initial calculations show that block level parameters for second order are achievable.
- Decreased complexity of second order modulator makes it a logical choice.

OVERSAMPLING RATIO M=80
SIMULATED IDEAL PEAK SNR= 76dB

METHODOLOGY

- By allocating $S_{QUANT} = S_{ELECTRONIC} = 2kT/CM$, we set constraints for the minimum size capacitors and electronic noise of the opamp. By MIΔΑΣ simulations, we choose the ratio of range of the opamp outputs with respect to Δ, so that the effect is less than 1-2dB drop of the SNDR.
- By hand calculations we set constraints for the block level parameters.
- We use the results of the hand calculations as initial values for MIDAS and we iterate until the constraints generated are feasible and allow of a margin at least 3-4dB to account for other nonidealities. The nonidealities simulated with MIDAS are only the ones that have been shown in theory to have considerable effect on the performance.

HIGH LEVEL INTEGRATOR CONSIDERATIONS

- ***OUTPUT RANGE***: DR > 1.5Δ from MIDAS . Use 1.7Δ for safety
- CHOOSE Δ=3 V , RANGE = 5.1V
- ***FINITE AMPLIFIER GAIN*:** Ho > 300

$$H_o > M^{5/4} \qquad ,(L = 2)$$

- ***SLEW RATE*:** SR > 2Δ/Ts from MIDAS. Use 3Δ/Ts .
- ***BANDWIDTH***: fu > 2Ts.
- ***RC CONSTANT OF SWITCHES*** : Tradeoff between settling and charge injection. Charge injection can be due to mismatch of switches.
- ***kT/C NOISE***: Small. Capacitor size set by charge injection.
- ***ELECTRONIC NOISE*** : Flicker noise of first integrator dominant. Thermal noise small.

- ***INTEGRATOR NONLINEARITY:*** Due to capacitor voltage dependence and nonlinearity of amplifier gain. THD < 0.03%

SAMPLING JITTER : Δt < 200ps for B=500kHz

HIGH LEVEL COMPARATOR CONSIDERATIONS

- ***COMPARATOR HYSTERESIS*****:** Hysteresis < 0.1 Δ. Use 0.3 Δ.

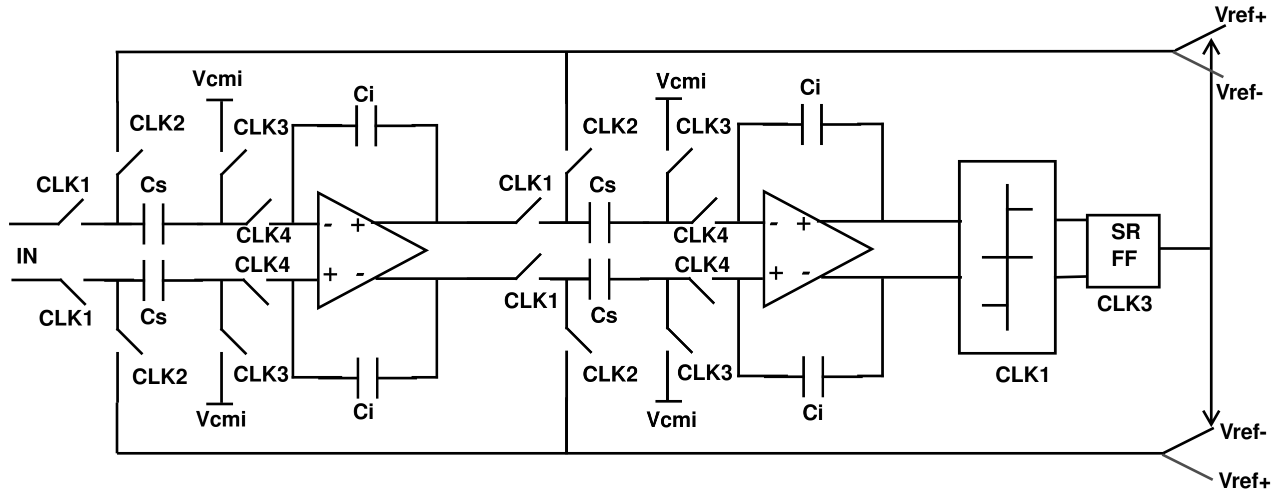
$$S_Q = \frac{\pi^{2L}}{2L+1}\left(\frac{1}{M}\right)^{2L+1}\Delta^2\left[\frac{1}{12}+4h^2\right]$$

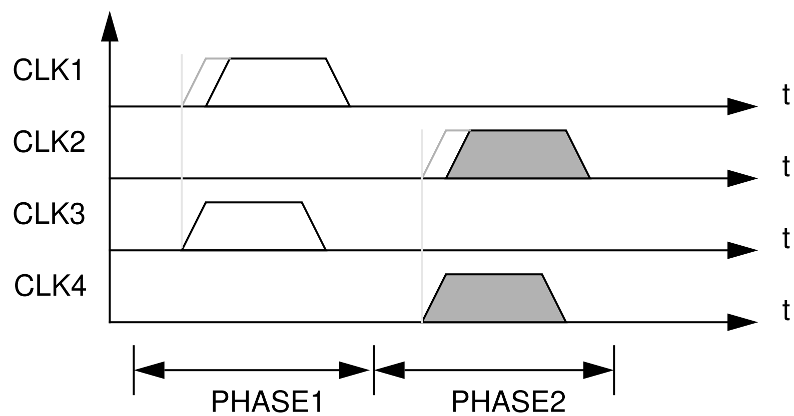
- ***SPEED*****:** Comparison must be made within Ts/2. Design for Ts/4.
- ***OFFSET, NOISE*****:** Not critical due to high gain negative feedback loop.

HIGH LEVEL CONSTRAINTS

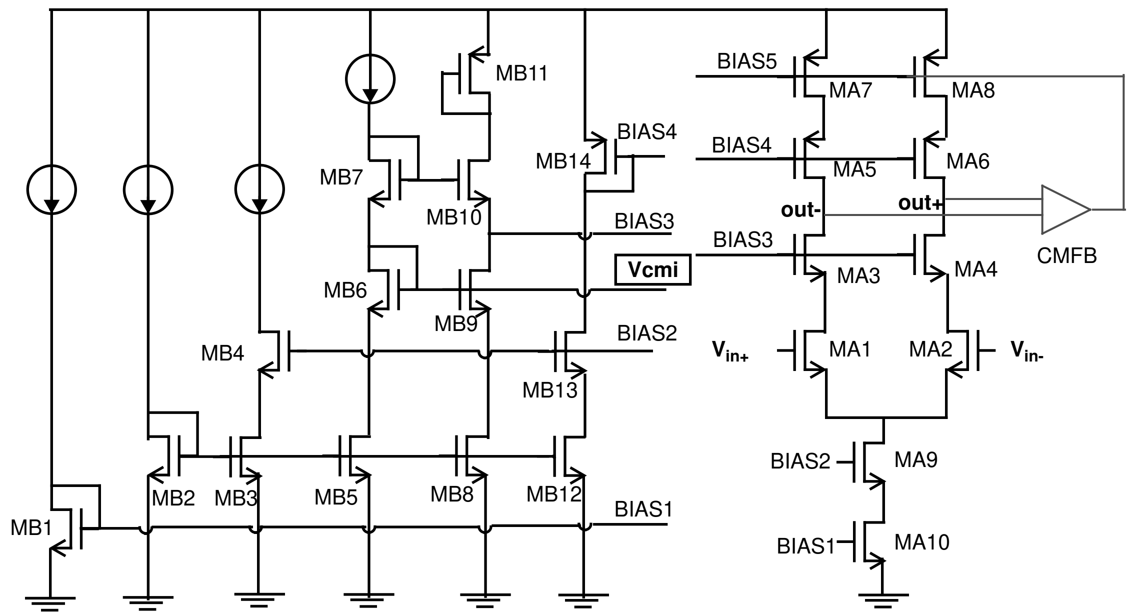
Constraint	Value	Constraint	Value
M	80	Offset	<90mV
Δ FULL SCALE	3V	Input + kT/C noise	<200µV
OPAMP DC GAIN	>300	Switch RC time constant and integrator setlling	< 6ns
GBW	>160MHz	Comparator speed	<3ns
SR	> 720V/µs	Comparator Hysteresis	<100mV
DR	5.1	Sampling Jitter	<200ps
Opamp THD for full scale inpuit	<0.03%		

IMPLEMENTATION: CIRCUIT TOPOLOGY





OPAMP IMPLEMENTATION : TELESCOPIC AMP



$$f_u = \frac{g_{mA1}}{C_l} = \sqrt{2K\frac{W}{L}I_{bias}} \qquad f_{p2} = \frac{g_{mA3}}{C_{A3}} = \frac{\mu_p \cdot (V_{gs} - V_t)}{2\pi L^2}$$

$$A_{dc} = \frac{g_m^2}{g_o^2} \qquad SR = \frac{2I_{bias}}{C_l}$$

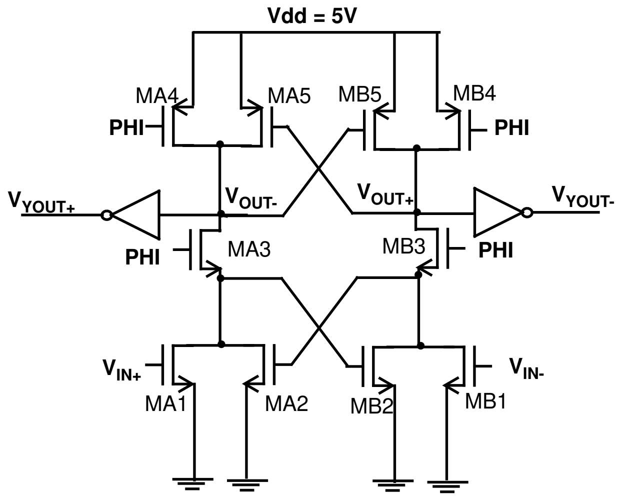
TRANSISTOR SIZES FOR AMP AND BIAS

MB1	55/1.5	MB8	4/3	MA1	85/1.5	MA8	200/1.5
MB2	2/3	MB9	55/1.5	MA2	85/1.5	MA9	250/1.5
MB3	8/3	MB10	55/1.5	MA3	85/1.5	MA10	250/1.5
MB4	55/1.5	MB11	100/1.5	MA4	85/1.5		
MB5	4/3	MB12	55/1.5	MA5	200/1.5		
MB6	55/1.5	MB13	55/1.5	MA6	200/1.5		
MB7	11/1.5	MB14	26/1.5	MA7	200/1.5		

PERFORMANCE SUMMARY

PERFORMANCE SPECIFICATION	SPECIFICATIONS	SLOW PARAMETERS	NOMINAL PARAMETERS	FAST PARAMETERS
GBW (MHz)	>200	206	272	350
DC GAIN	>300	460	620	870
PM (DEG)	>60	64	66	67
OUTPUT SWING (V)	>5	5	6	6.9
INPUT NOISE (0-500kHz) (uV)	<100μv	78	75	70
DISTORTION(*)	<0.03|%	0.02%	0.024%	0.026%
SETTLING TIME(**) (nsec)	<6nsec	6	5	4.5
POWER (mW)	-	4.75	5.42	6.1

FULLY DIFFERENTIAL POSITIVE FEEDBACK COMPARATOR



$$t_{delay} = \tau \cdot ln\left(\frac{V_{FS}}{V_{i,\,min}}\right)$$

$$V_o(t) = V_i(0) \cdot e^{t/\tau} \qquad ,\tau = \frac{C}{(g_{m,\,nmos} + g_{m,\,pmos})}$$

COMPARATOR DEVICE SIZES

MA1	36/1.5	MB1	36/1.5	INVERTER	
MA2	36/1.5	MB2	36/1.5	MNMOS	36/1.5
MA3	36/1.5	MB3	36/1.5	MPMOS	72/1.5
MA4	72/1.5	MB4	72/1.5		
MA5	72/1.5	MA6	72/1.5		

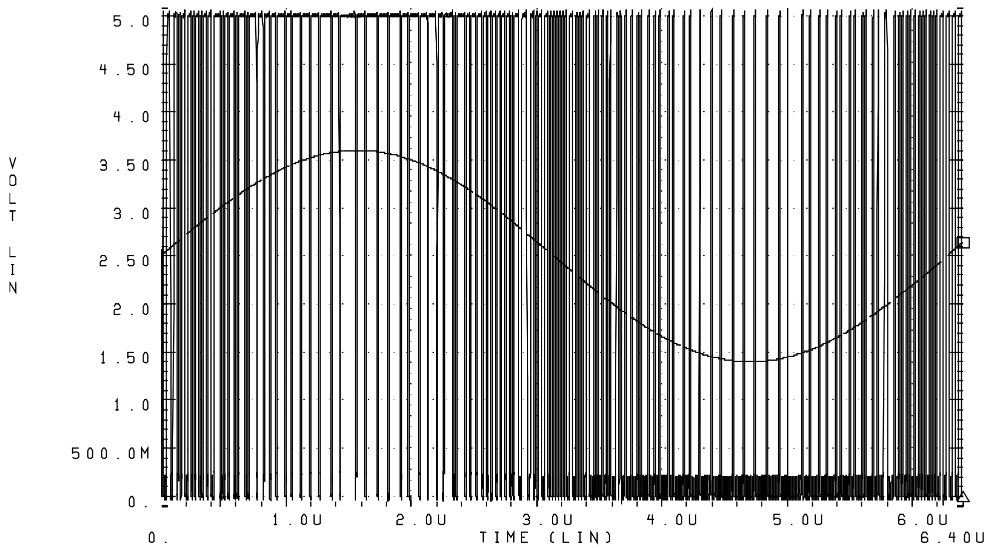
PERFORMANCE SUMMARY

Specification(NOMINAL)	Value
Resolution	50mV
Speed	3ns
Average Power	0.4mW

SPICE SIMULATION AND VERIFICATION

- Entire circuit simulated with SPICE
- Due to the large files generated by SPICE during the transient analysis and the long simulation time, only one cycle of a sine wave is used as input.
- We can only see the output of the modulator which tracks the input value.
- SNR calculations could not be performed due to the limited signal processing functions in SPICE.

SPICE MODULATOR OUTPUT



- 159.3KHz sine wave input of amplitude 1.1V.

SUMMARY OF RESULTS

Peak SNDR	74 dB
DR	81 dB
Quantization Noise	93uV
KT/C noise	22uV
Opamp thermal noise, flicker noise over bandwidth of 500kHz	77uV
Total gate area	~8300um^2
Power (**)	11mW
Supply	5V

CONCLUSIONS

- Second order sigma delta A/D design met all specifications.
- The design was verified by MIDAS simulation and to a lesser extent by SPICE simulation.
- Most parameters were overdesigned and therefore should be able to accomodate a higher oversampling ratio of M=128.

SO IT WORKS !! WE HOPE....