Top-Down, Constraint-Driven Design Methodology Based Generation of a Video Driver System

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Outline

- ➡ **Background on Top-Down Design Methodology**
- Video Driver Design
  - High Level Design
  - Circuit Level Design
  - Layout
  - Experimental Results
- Summary - Future work

Motivation

- Analog often is the bottleneck for large mixed-signal systems
  - non systematic, more intuitive
  - time consuning

➡ **We propose top-down methodology**
  - help analog designer, not substitute
  - hierarchical approach
  - provide rigorous tools at every level of hierarchy

Key points of the Methodology

- Start with system architecture and constraints
- Choose architecture of components
  - High level simulation
- Propagate constraints from current to next
  - Behavioral Simulation
  - Optimization
- Repeat process until done
  - library component, module generator, transistor level design
- Constraint -driven physical synthesis
- Verify design bottom-up
  - Extraction
  - Hierarchical simulation

Advantages

- Systematic
- Efficient exploration of design space
- Early verification (behavioral simulation)
- Guaranteed feasibility
- Reduces overdesign
- Costly low-level design iterations can be avoided
- Fast verification
- Speed up design cycle

Why this design example

- Prove the methodology for higher complexity systems

Methodology definition (H. Chang,et al cicc 92) → DACs (H. Chang et al cicc 94) / Σ–Δ A/D (H. Chang et al cicc 95) → Video System (This work) → RF receiver

- Popular design example
- Integrate programmable PLL frequency synthesizer

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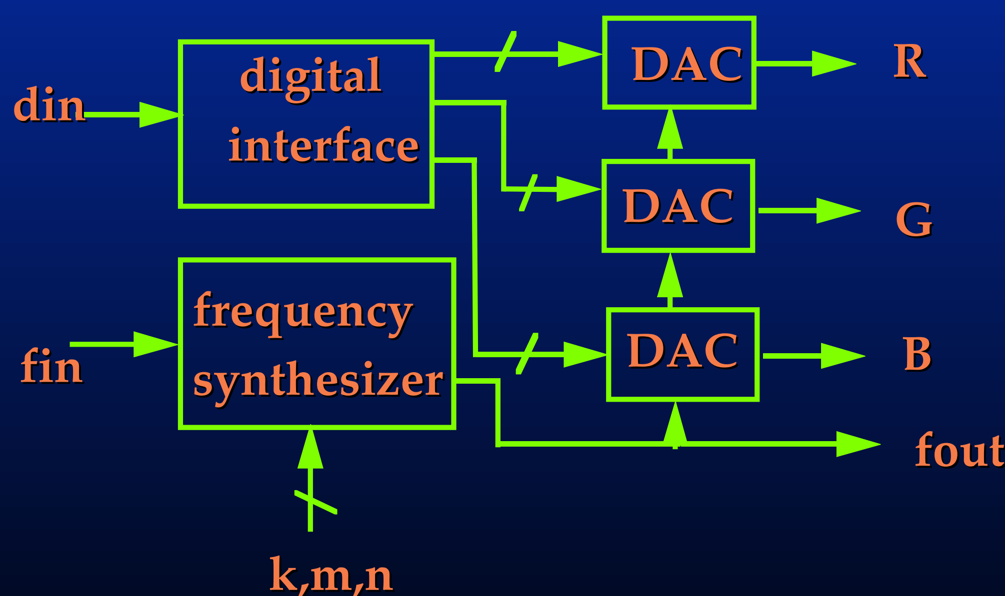
Video Driver System

- Integrate 3 DACs for the R, G, B signals plus programmable frequency synthesizer



Performance:
25MHz - 135MHz
jitter < 1 %

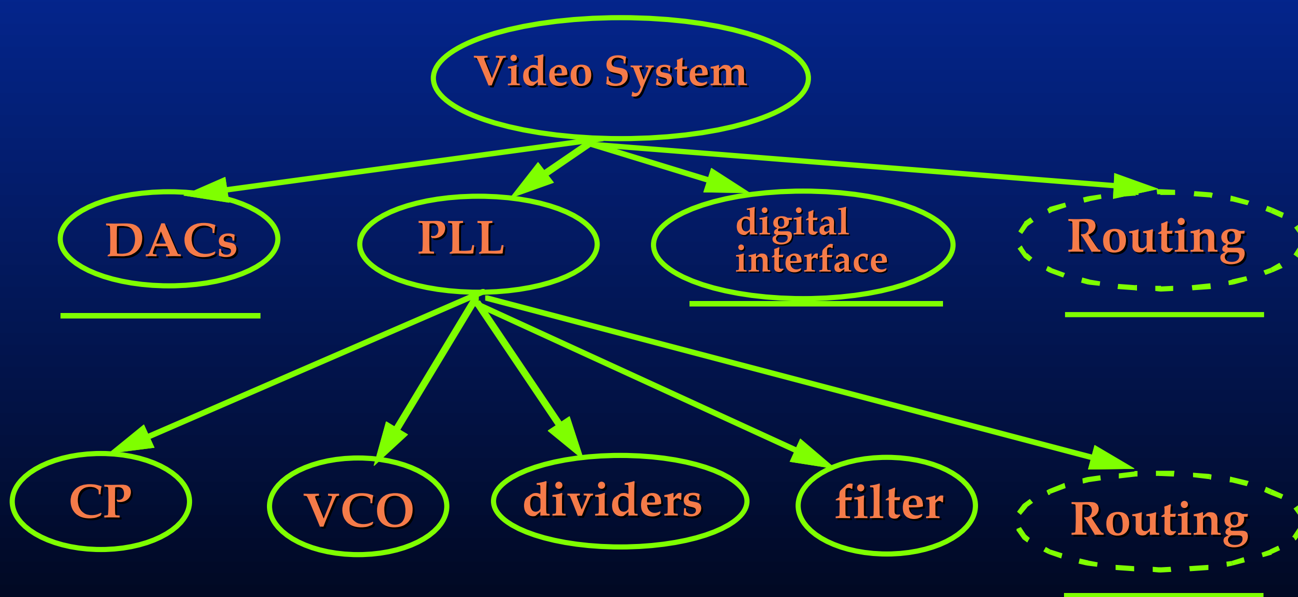
Supply:
5V

Technology:
MOSIS HP 1.0u

Power:
minimize

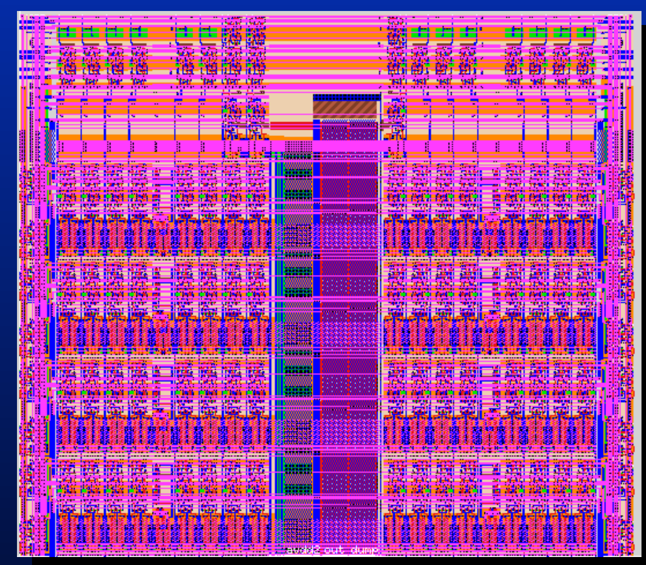
High Level Decomposition

- For the DACs. module generators are used
- PLL frequency synthesizer: all the way to layout



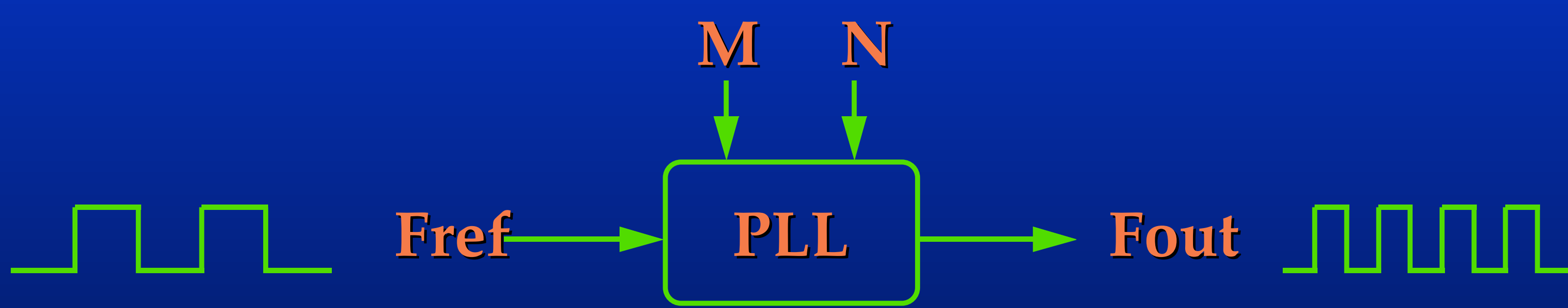
Video Driver System
D/A converter synthesis

- Specifications
  - resolution: 8 bits
  - INL, DNL: 1LSB
  - Speed: 150MHz
- Use module generator for current source, interpolative DAC
  - ~1.5 CPU hours in alpha



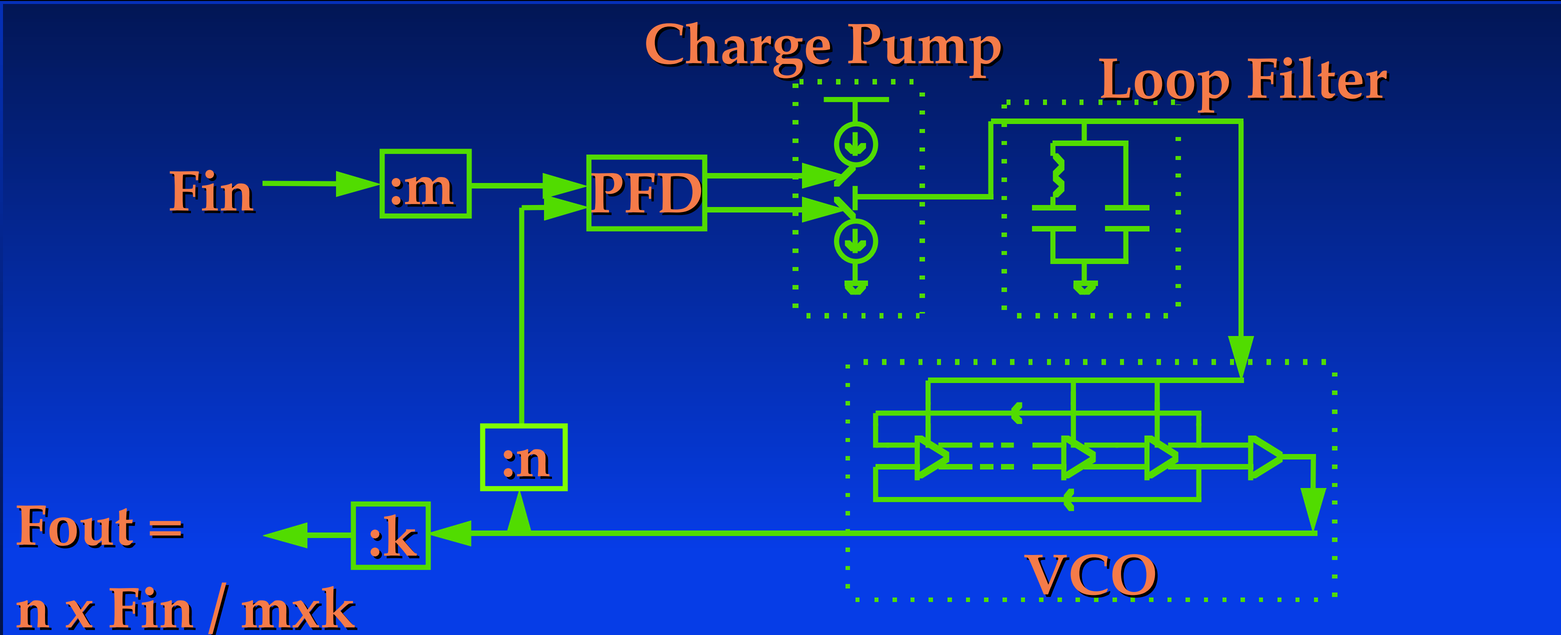
R. Neff et al CICC '95

Video Driver System Frequency Synthesizer



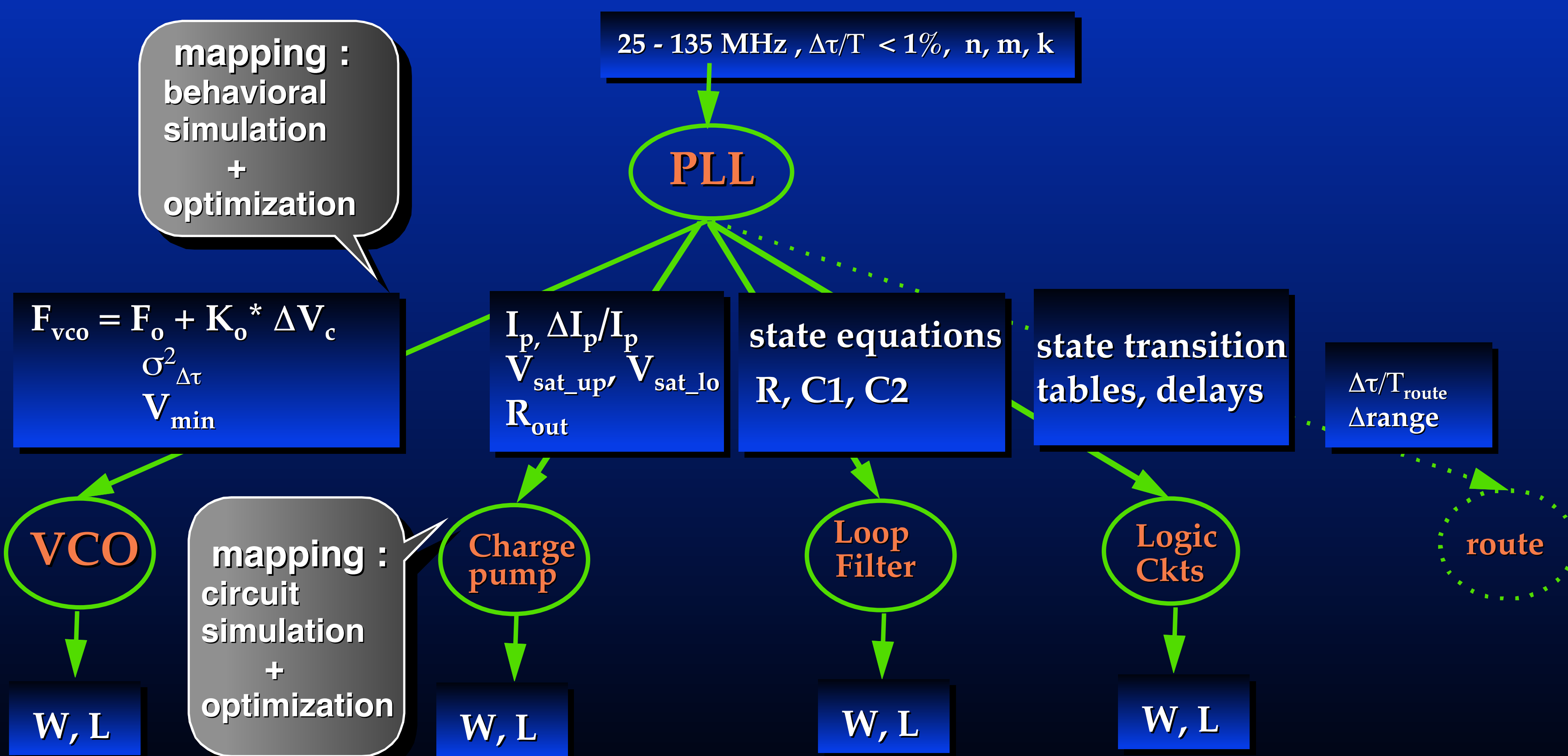
- Goal: Design a programmable frequency synthesizer for a Video Driver system
- Architecture selection
  - behavioral simulation
  - optimization

Architecture Selected: PLL



- Charge-Pump PLL with ring oscillator VCO
- Fixed F_{ref}, m, n, k to produce given frequencies

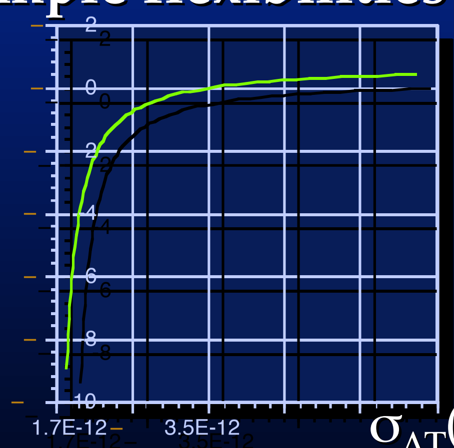
Hierarchical Decomposition/Mapping: PLL



High Level Optimization - 0bjective

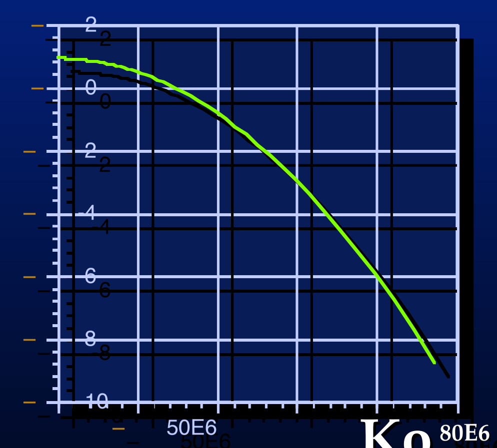
- flexibility(Ko , $\sigma^2_{\Delta\tau}$, R , C , Ip) = f(Ko) + g($\sigma^2_{\Delta\tau}$) + h(R) + i(C) + j(Ip) + ...
- Flexibility functions based on design experience and circuit equations
- Example flexibilities :

g($\sigma_{\Delta\tau}$)



$\sigma_{\Delta T}$(VCO)

f(Ko)



Ko

High Level Optimization - Problem Formulation

$$\begin{aligned}
\max \quad & \text{flexibility}(R, C, C_1, I_p, K_O, \ldots) \\
s.t. \quad & \Delta T / T_{100\text{MHz}} \le 0.7\ \% \\
& PM_{PLL} \ge 45^{O} \\
& R_L \le R \le R_U \\
& \vdots \\
& K_{OL} \le K_O \le K_{OU}
\end{aligned}$$

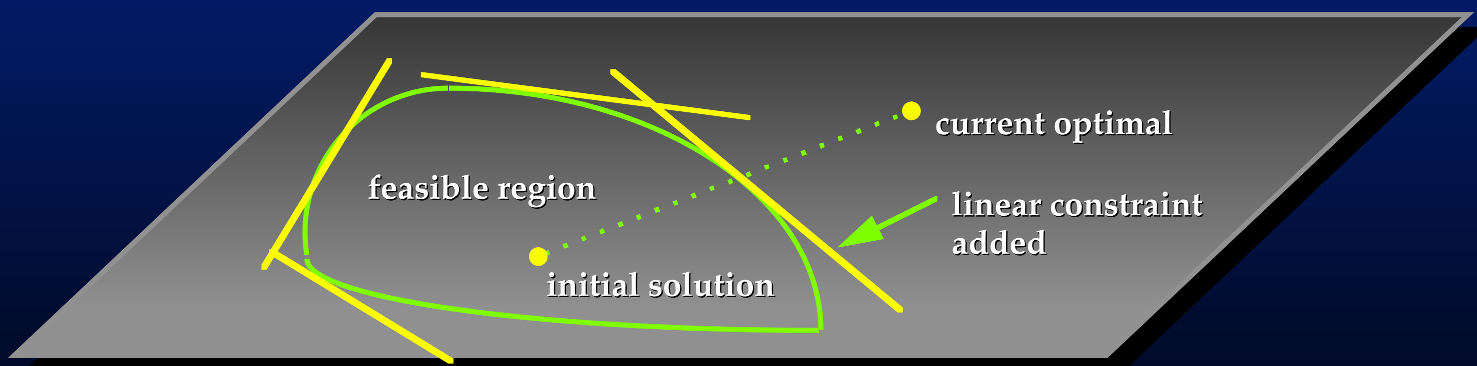
Constants

Fo	100 MHz
V_{sat_up}	4.8 V
V_{sat_lo}	0.2 V
$\Delta I_p/I_p$	5 %
R_{out}	2 MΩ
V_{min}	1.8 V

- **Jitter simulation**
  - Check worst cases for stability
  - Computes jitter if stable
  - Uses behavioral simulation tool (A. Demir et al CICC94)
- **Phase margin > 45° : parameter variations**
  - Computed analytically

High Level Optimization - Algorithm

- Most non-linear optimization algorithms require accurate calculation of 1st and 2nd derivative
- Timing jitter is the result of a Monte-Carlo Simulation - hard to have accutate derivatives
- Method used: Supporting Hyperplane requires 1st derivative information only - gives results even with noisy gradients.



➡ requires convexity

High Level Optimization - Results

objective
flexibility = 2.79

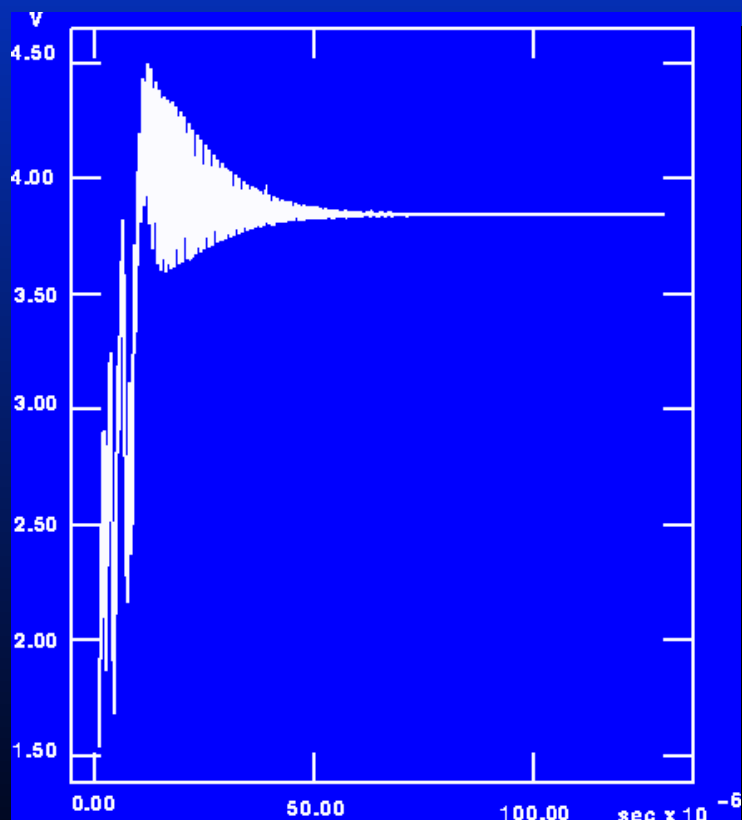
constraint	value
$jitter_{140MHz}$	0.7%
phase margin	44^{O}

Parameter	Value
R	200.5k
C	57.8pF
C1	5pF
Ip	15.8uA
$\Delta\tau_{VCO}$ (140MHz)	3.33ps
Ko	40MHz/V

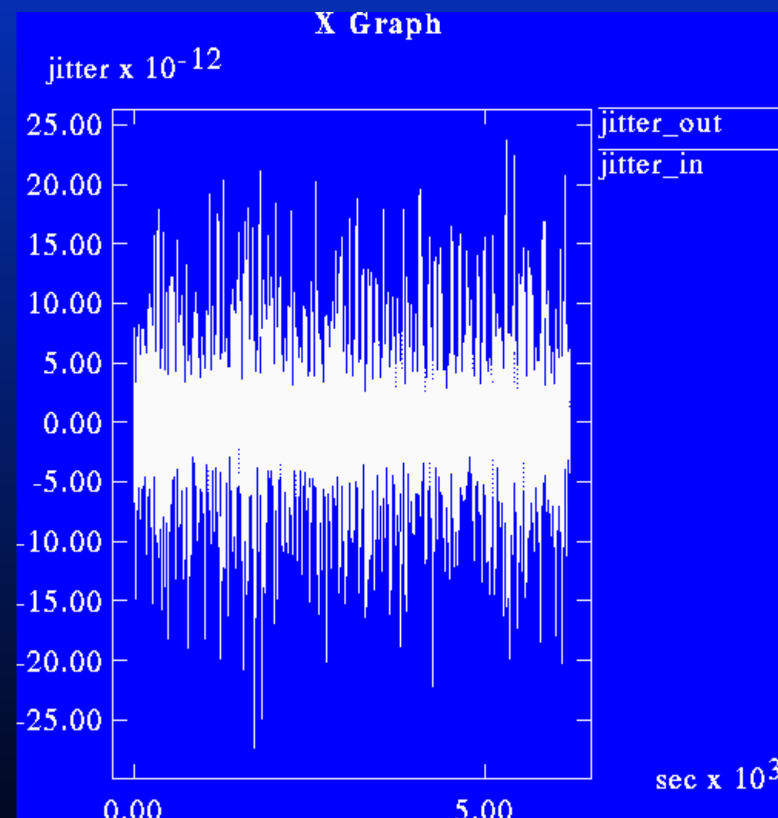
Iterations	8	
CPU	7600 sec	(DEC Alpha)

- Tolerance to parameter variations verified

High Level Optimization - Results



Transient response



Jitter simulation

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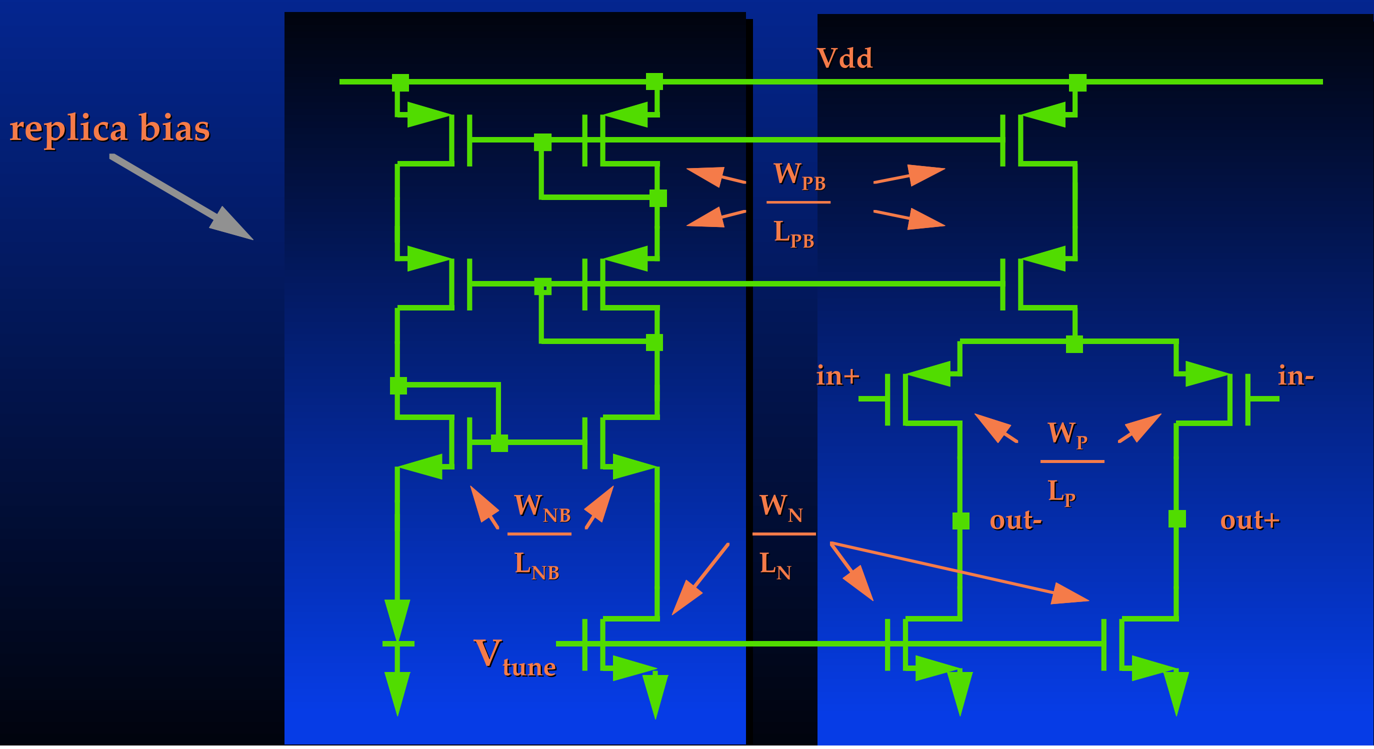
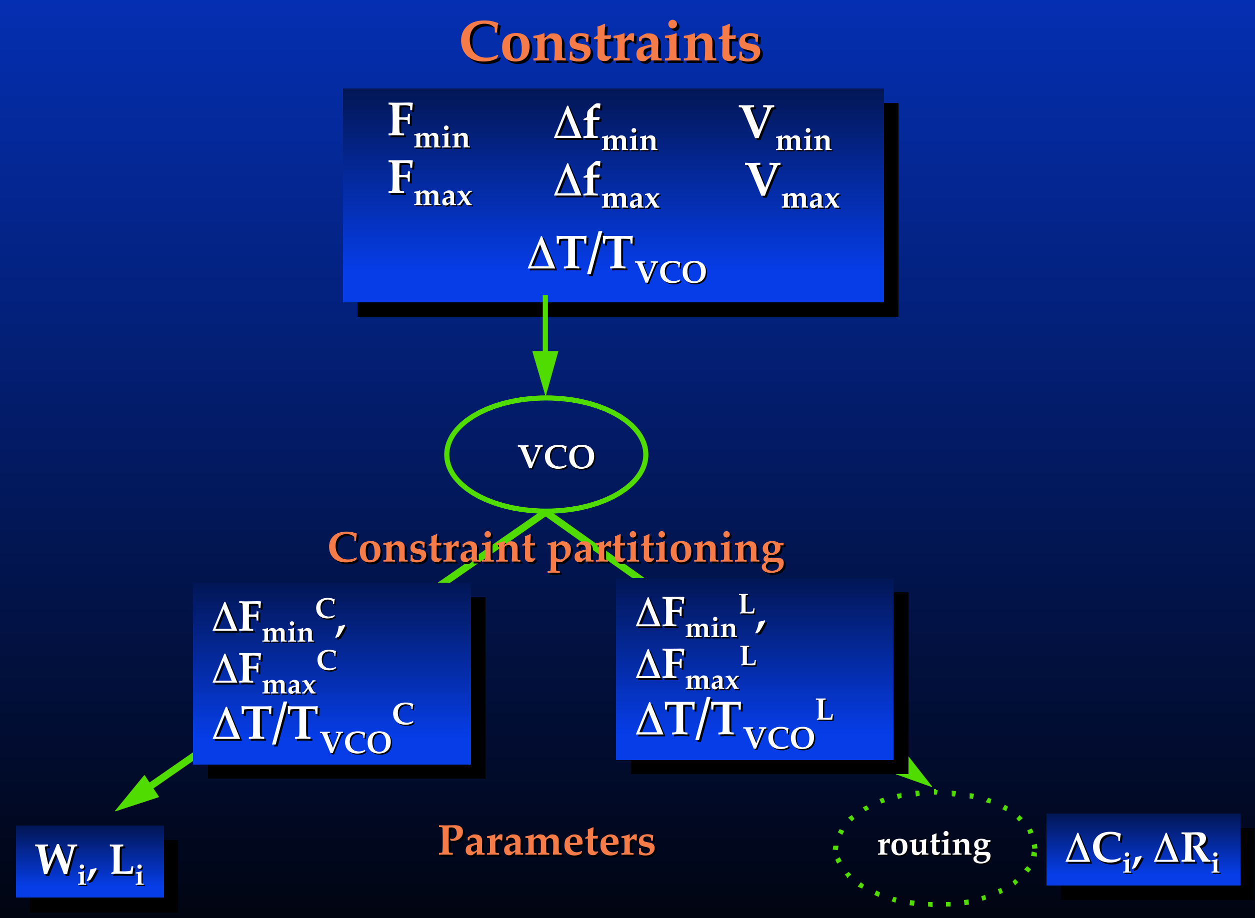
VCO Topology

- 8 stage ring oscillator VCO
- use differential cells to reject supply noise



(similar to D. Reynolds ISSCC 94)

VCO decomposition



Low Level Optimization - VCO

$$
\begin{aligned}
\min \quad & Power(Wi, Li, \ldots) \\
s.t. \quad & \Delta T_{VCO\,140\,MHz} \le 3ps \\
& F_{MAX} - \Delta F_{MAX} \le F_{MAX} \le F_{MAX} + \Delta F_{MAX} \\
& F_{MIN} - \Delta F_{MIN} \le F_{MIN} \le F_{MIN} + \Delta F_{MIN} \\
& V_{MIN} \le V_1 , \quad V_2 \le V_{MAX} \\
& \boxed{\left[S_C^P \right]^T \bullet \Delta C_{max} \le \Delta P_{max}} \\
& Wi_L \le Wi \le Wi_U , \; Li_L \le Li \le Li_U
\end{aligned}
$$

Constants

L_{nb}, L_{pb}	1 u
W_{pb}	20 u
W_{nb}	10 u
ΔC_{Lmax}	50 %
ΔC_L	15 fF

- **Fmin, Fmax: simulation**
- **ΔT_{VCO} :equations**
- **Algorithm : Supporting Hyperplane**

Key idea **use sensitivities and parasitics estimate**

VCO Optimization - Results

Performance

- Fmax = 163MHz
- Fmin = 48MHz
- Jitter = 1.5 psec @140MHz
- Power = 6.2 mW

Variables

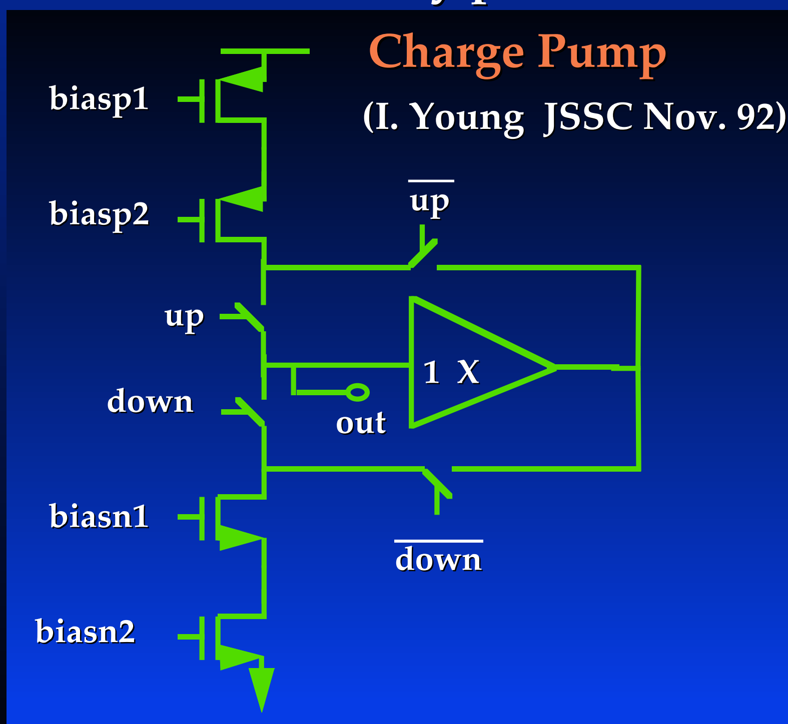
Wn	2.6u
Ln	4u
Wp	36u
Wp	1u

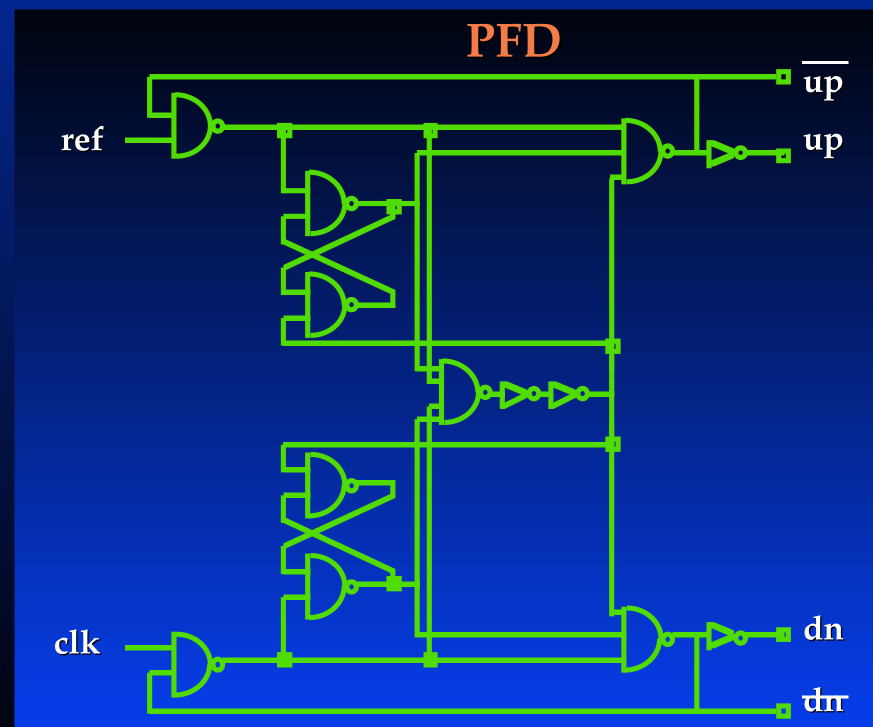
4 Iterations

2070 CPU sec (DEC Alpha)

Low Level Decomposition

- Other cells: automatic layout generation or standard cell techniques
  - Verify performance





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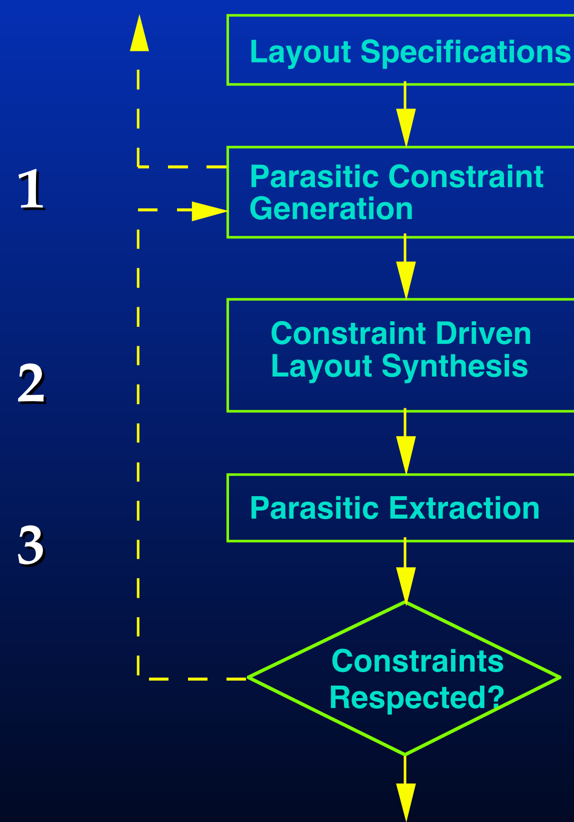
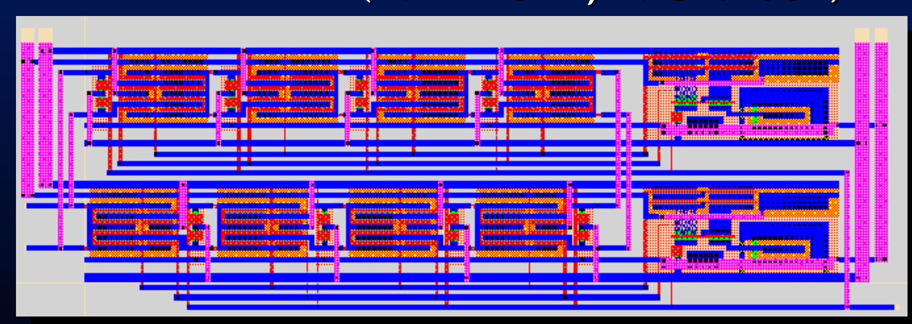
Layout Design Flow



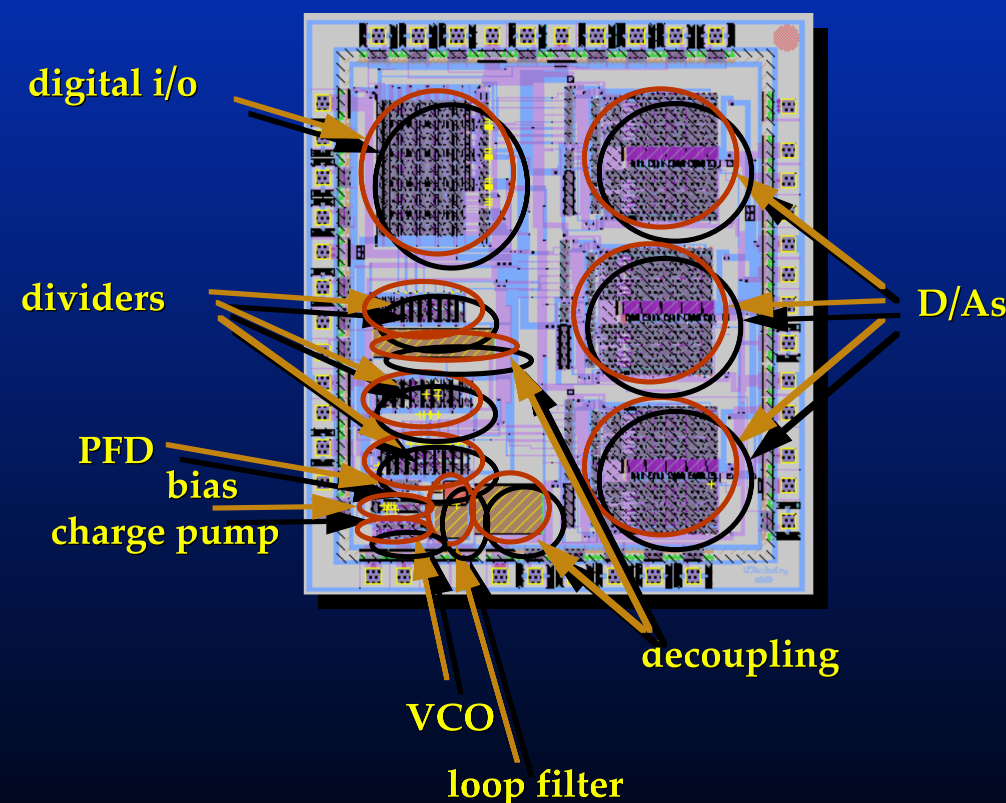
- Module Generation: VCO
  - Fully parametrized
  - All bus sizes adjustable
  - Fully scalable
  - Fixed floorplan
- Under development
  - Substrate noise aware layout

(P. Miliozzi, E. Charbon)



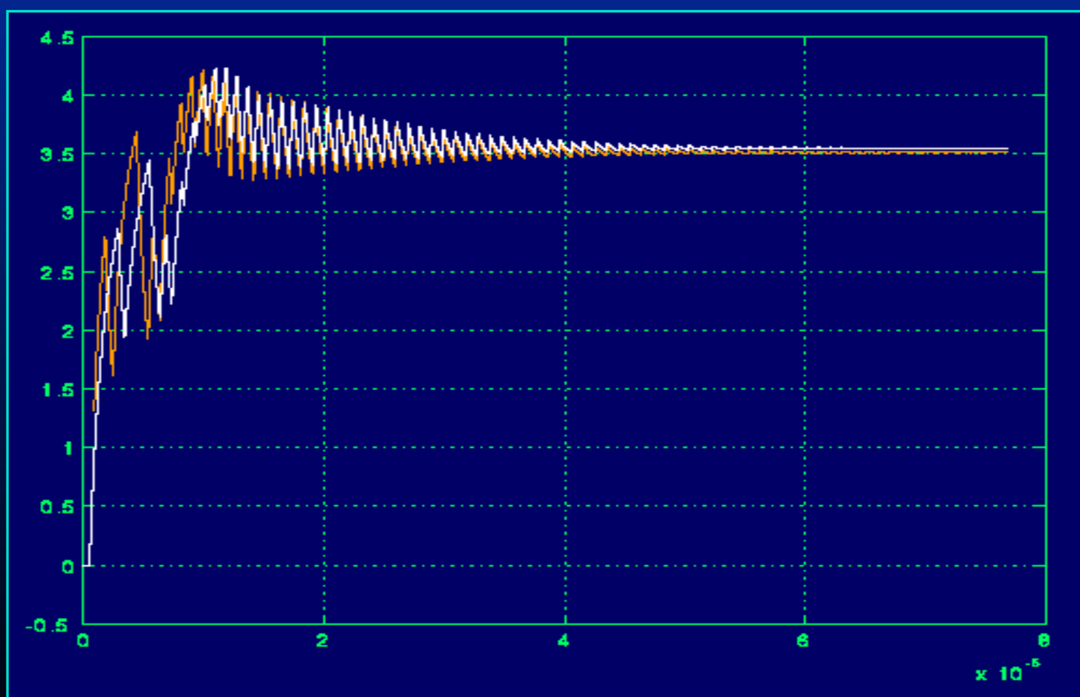
Video Driver Layout

- ~20,000 transistors
- used OCTTOOLS for automatic routing
- total area: 3.4mm x 3.9mm



Bottom-up Verification

- Bottom-up verification performed
  - individual components at circuit level
  - PLL using behavioral simulation with extracted parameters



SPICE :
20 CPU hours

Behavioral Simulation :
250 CPU secs

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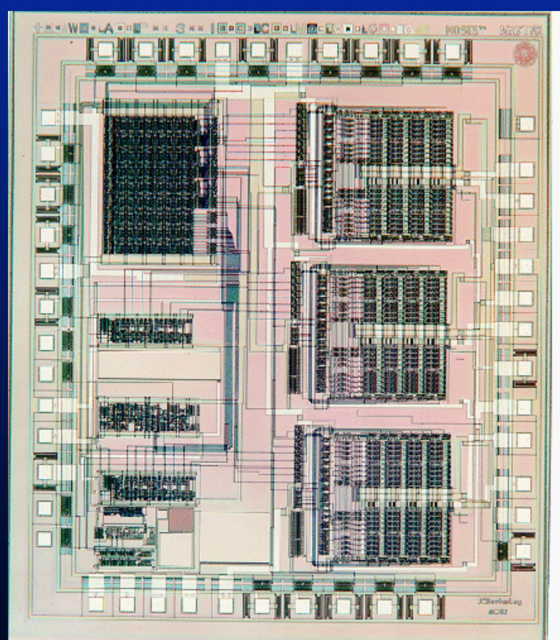
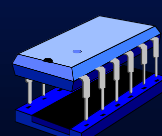
Experimental Results

Chip fabricated using 1.0u HP process





Measurements

D/A

- INL 0.15 LSB
- DNL 0.05 LSB
- Settling time (2%) 6ns

PLL

- Range 5Mz - 125MHz
- Jitter 0.5% (100MHz)

System

- To be tested together with monitor

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➡ **Summary - Future work**

Summary - Future work

- Developed techniques to apply top-down methodology in a more complex system
- Complete desing example from specifications to working fabricated parts
  - hierarchical approach
  - behavioral simulation
  - optimization
  - bottom-up verification

- Apply methodology and expand use to other designs
  - RF systems