Use of Sensitivities and Generalized Substrate Models in Mixed-Signal IC Design *

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Abstract

A novel methodology for circuit design and automatic layout generation is proposed for a class of mixed-signal circuits in presence of layout parasitics and substrate induced noise. Accurate and efficient evaluation of the circuit during design is possible by taking into account such non-idealities. Techniques are presented to derive and use a set of constraints on substrate noise and on the geometric instances of the layout. Verification is performed using substrate extraction in combination with parasitic estimation techniques. To show the suitability of the approach, a VCO for a PLL has been designed and implemented in a CMOS $1\mu m$ technology. The circuit has been optimized both at the schematic and at the layout level for power and performance, while its sensitivity to layout parasitics and substrate noise has been minimized.

1 Introduction

In recent years, analog and mixed-signal integrated systems have grown in size and complexity with an increasing need for implementing new and more complex functions. In a typical communication chip for example, antennas, radio-frequency components, analog and digital subsystems have to be designed in a unified way to provide performance, power and size needed by the application. In general, designing high-performance analog components is time-consuming, often resulting in the bottleneck for the whole design.

Digital sections of the chip are, to a large degree, relatively immune to various noise sources inherent to integrated circuits. Analog circuits, on the contrary, are generally sensitive both to thermal and electrically induced switching noise. Switching noise is mainly transmitted from digital to analog sections through power supply rails and substrate. For this reason, great effort has been devoted to the analysis and modeling of substrate-related parasitics in mixed-signal circuit design [1, 2, 3, 4]. These methods are well suited for the evaluation of circuit performance after the physical assembly. However often *a priori* knowledge of circuit parasitics is needed to optimize performance, area or power at both design and layout implementation level.

A behavioral-based constraint-driven approach to the design and physical assembly of mixed-signal ICs has been proposed in [5]. In this approach, a top-down hierarchical decomposition of the circuit is used to characterize the behavior and allow early verification and failure detection at each stage of the design. Performance specifications are mapped onto constraints which are used at the next level of hierarchy for a behavioral- or SPICE-based optimization. Design decomposition has the main advantage of partitioning a complex design into a set of simpler problems which can be solved independently. A test case of a Phase Locked Loop (PLL) has been considered to describe our approach.

In this paper, models and optimization techniques have been extended to include the effects of parasitics and substrate noise. A methodology is described for generation and enforcement of constraints on interconnect parasitics and substrate noise. Worst-case sensitivities are used to evaluate performance degradations due to these non-idealities. Substrate noise is characterized by use of process-independent *local noise generators* and detailed substrate resistance extraction. The advantages of this technique are manifold. Firstly, constraints can be derived once for a given design, while only a simple parasitic estimation is needed for their enforcement. Secondly, no assumptions are required on the waveform and/or distortion levels through the substrate. Finally, several trade-offs are possible during the physical assembly between power and performance by different budgeting of maximum allowed parasitics and noise figures.

The paper is organized as follows: in Section 2 a behavioral model for the PLL is described and the benefits of using sensitivity analysis during the optimization steps are discussed. Techniques to address the substrate noise analysis through the use of sensitivities are introduced in Section 3. In Section 4 a complete substrate characterization is given and techniques for substrate noise extraction using a novel partitioning method of the noise sources are proposed. Finally in Section 5 the suitability of the approach is shown through a realistic PLL design.

2 Parasitic-Aware Optimization

Modeling Critical Components

The first step in a top-down constraint driven design methodology consists of the characterization of the analog blocks through behavioral

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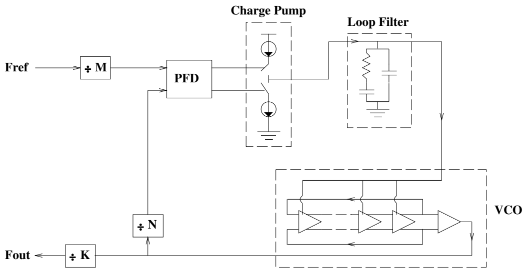

Figure 1: PLL Block Diagram.

modeling. The architecture used as a basis for the PLL design is shown in Figure 1. It consists of a crystal reference frequency generator (F_{ref}), a phase-frequency detector (PFD), a charge-pump, a second order RC loop filter and a voltage controlled ring oscillator (VCO) [6, 7]. The output frequency is expressed as $F_{out} = F_{ref} \cdot n/mk$, where n, m and k represent the dividing ratios of the frequency scalers in Figure 1.

Each of the PLL blocks is characterized by a set of behavioral parameters. The PFD is characterized by a state transition table and a delay, the dividers by a delay and a divide ratio. The loop filter is determined by its component values R, C_1, C_2, the charge pump by its bias current I_{cp} and output resistance R_{out}. The VCO's frequency-to-voltage characteristic can be significantly affected by process, temperature variations and layout parasitics. Since we have no control on process and temperature variations, the PLL is optimized in such a way that performance degradation due to these non-idealities is kept within pre-determined tolerances.

The jitter performance of the system is mostly affected by the jitter of the VCO. Sources for VCO jitter are thermal noise and coupling of digital noise from the supply and the substrate. In this work we focus on the effect of the substrate coupling to the peak-to-peak jitter. The VCO model used is defined by the following equation:

$$F_{out} = F_0 + K_0 \cdot \triangle V \ , \tag{1}$$

where F_0 is the VCO central frequency of operation, K_0 the frequency-to-voltage gain, $\triangle V$ the deviation of the applied voltage in the control node from the nominal. Performance constraints for the PLL are:

1. stable frequency range of operation: $F_{min} \leq F_{out} \leq F_{max}$;
2. peak-to-peak timing jitter of the generated clock: $J_{pp} \leq \overline{J}_{pp}$.

This model was used by the behavioral simulator described in [8] to execute worst-case performance analysis.

In order to proceed with the top-down approach it is necessary to map these specifications onto lower-level constraints on the physical implementation.

Parasitic Constraint Generation

Let us consider a performance set represented by vector $\mathbf{K} = \left[K_1, K_2, \cdots, K_{N_k}\right]^T$. We denote the maximum allowed performance degradation by vector $\overline{\triangle \mathbf{K}}$ and the parasitics, with nominal zero value, by vector $\mathbf{P} = \left[P_1, P_2, \cdots, P_{N_p}\right]^T$. The constraint vector $\mathbf{P}^{(bound)}$ is defined so that

$$p_j \leq p_j^{(bound)} \ \forall j = 1, \cdots, N_p \ \Rightarrow \ \triangle K_i \ \leq \ \overline{\triangle K_i} \ \forall i = 1, \cdots, N_k,$$

where $\triangle \mathbf{K}$ is the vector of performance degradations. Finally two vectors $\mathbf{P}^{(max)}$ and $\mathbf{P}^{(min)}$ are defined to delimit the space where

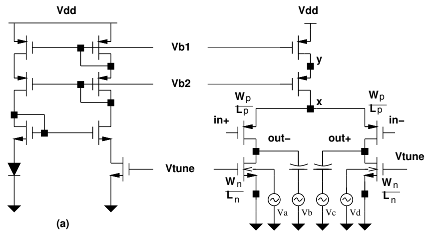

Figure 2: VCO basic components: (a) bias cell, (b) fully differential inverter.

Performance	Nominal	Max. Variation
K_0	$40MHz/V$	$4MHz/V$
F_0	$100MHz$	$10MHz$
J_{pp}	0	1%

Table 1: Performance constraints obtained by the behavioral optimization of the VCO.

the constraint vector can be chosen. This space is called *feasibility region*. Assuming parasitics are small, we can linearize a performance function around its nominal value. The sensitivity vector $\mathbf{S}_{\mathbf{P}}^{K_i}$ of K_i with respect to parasitics $\mathbf{P}$ is defined as

$$\mathbf{S}_{\mathbf{P}}^{K_i} = \left[\left.\frac{\partial K_i}{\partial P_1}\right|_{P_1=0}, \left.\frac{\partial K_i}{\partial P_2}\right|_{P_2=0}, \cdots, \left.\frac{\partial K_i}{\partial P_{N_p}}\right|_{P_{N_p}=0} \right]^T ,$$

hence, performance degradation $\triangle K_i$ can be represented in terms of sensitivities [1] as

$$\triangle K_i = \left[\mathbf{S}_{\mathbf{P}}^{K_i}\right]^T \cdot \mathbf{P} \ . \tag{2}$$

The constraint generation problem can be mapped onto a constrained optimization problem, where the objective is the flexibility of the physical realization provided that the maximum performance degradation due to parasitics meets specifications. Flexibility functions give a measure of the level of difficulty in implementing a particular layout structure to obtain a performance. In our approach a quadratic flexibility function has been used as described in detail in [9].

Design Optimization Techniques

The robustness of the design can be significantly improved by use of sensitivity analysis applied to circuit performance.

In our top-down design methodology an optimization step is used for the selection of the parameters of each building block so as to meet all performance constraints at the higher level of the hierarchy [5].

In the case of the VCO shown in Figure 1, the performance constraints obtained from behavioral optimization are listed in Table 1, where performance deviations do not take into account process gradients. The optimization problem for the VCO used in the PLL can be written as:

$$\begin{array}{ll} minimize & \text{Total Power}(W_p, L_p, W_n, L_n) \\ such\ that & F_{min_0} - \triangle F_{min_0} \leq F_{min} \leq F_{min_0} + \triangle F_{min_0} \\ & F_{max_0} - \triangle F_{max_0} \leq F_{max} \leq F_{max_0} + \triangle F_{max_0} \\ & J_{pp} \leq 1\% \end{array}$$

where W_p, L_p, W_n, L_n are the transistor sizes of the fully differential inverter, shown in Figure 2.

[1] The sensitivity has not been normalized following the notation in [9].

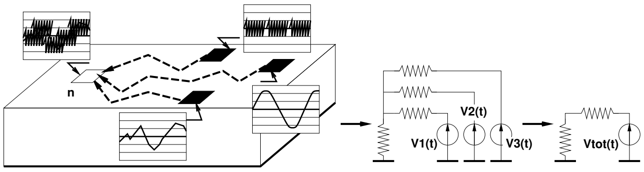

Figure 3: The principle and modeling of *local noise generators*.

This optimization minimizes current I through each VCO cell and therefore the size of the input transistors of the differential pair, which determine the cell delay, thus keeping the ratio I/C_{out} constant, where C_{out} is the capacitance at the output node of each cell. Reducing transistor sizes has the drawback of increasing the sensitivity with respect to parasitics. In fact C_{out} is given by the gate capacitance of the next cell input transistor and by parasitics. Hence, if the layout parasitics are not well controlled, a significant degradation of circuit performance could result. This can be avoided if the sensitivity information is used during the optimization process. The new optimization problem is rewritten as:

$$\begin{array}{ll} minimize & \text{Total Power}(W_p, L_p, W_n, L_n) \\ such\ that & F_{min_0} - \triangle F_{min_0} \leq F_{min} \leq F_{min_0} + \triangle F_{min_0} \\ & F_{max_0} - \triangle F_{max_0} \leq F_{max} \leq F_{max_0} + \triangle F_{max_0} \\ & J_{pp} \leq 1\% \\ & \left[\mathbf{S}_{\mathbf{P}}^{K_i}\right]^T \cdot \mathbf{P}^{max} \leq \overline{\triangle K_i} \;\; \forall i = 1, \cdots, N_k \;\; . \end{array}$$

Finally, let us consider the problem of enforcing a couple of constraints operating on the parasitic resistance and capacitance due to the same interconnection. These two parasitics depend simultaneously on wire dimensions (Width and Length) $R = \rho \, \frac{W}{L}$ and $C = C_0 \, W \, L$. The problem can be solved using the following algorithm:

EnforceConstraint{
set $W = W_{min}$ and $L = L_{min} \implies C = C_0 \, W_{min} \, L_{min}$
do{
evaluate $R = \rho \, \frac{W}{L}$
if $(R < R_{max})$ then exit the cycle
else $W = W + \triangle W$
} while $(C < C_{max})$
if $((C > C_{max})$ or $(R > R_{max}))$ then "infeasible" $\Rightarrow$ stop
else "constraint enforced"
}

where $\triangle W$ is the minimum increment (λ) allowed by process design rules.

3 Techniques for Substrate Noise Analysis

The use of sensitivities for the constraint generation problem can be extended to substrate noise analysis. Generally the substrate noise analysis is addressed in two ways: through a complete extraction of substrate's electrical properties [4]; using analytical approximation to derive a simpler model [2, 10]. Either technique has drawbacks, the first one in the computational complexity and the second one in the accuracy. Both share the dependence of simulation results on technology and on the physical implementation of the circuit, which might not be available at high-level design stages.

Constraint generation, in a strict sense, requires that parasitics be entities associated with one or more physical structures of the layout being made. To address this issue we introduce the concept of *local noise generator*. A local noise generator is defined as a model $G_n(t, \mathbf{\Pi})$ of the substrate noise present at node n, at time t. Vector $\mathbf{\Pi}$ represents all parameters relevant to characterize generator G_n at its nominal value. Due to the different nature of these parameters, $\mathbf{\Pi}$ can be split into basic components $\mathbf{\Pi} = \left[\mathbf{W}^T \, \mathbf{G}^T \, T \, V_0\right]^T$. $\mathbf{W}$ represents process-dependent and $\mathbf{G}$ layout-related parameters, T is the temperature and V_0 the local substrate potential. Variation vector $\triangle\mathbf{\Pi}$ represents all variations of these parameters from nominal.

Bounds on all parameter variations in $\triangle\mathbf{\Pi}$ can be derived based on sensitivities and constrained optimization. Let $\mathbf{S}_{\mathbf{\Pi}}^{K_i}$ be the sensitivity vector, then the i-th performance variation $\triangle K_i$ can be expressed as:

$$\triangle K_i = (\mathbf{S}_{\mathbf{\Pi}}^{K_i})^T \cdot \triangle\mathbf{\Pi} \, . \tag{3}$$

Due to the mechanism of noise modeling obtained using local generators, constraints on noise parameters can be derived independently of a particular IC process. Hence, the constraint generation needs to be repeated *only once* for a given circuit. During layout synthesis, process-dependent substrate extraction methods are used to enforce bounds.

From a theoretical point of view each generator could be supplied by a different signal waveform. However, since the size of the analog section of a mixed-signal circuit is generally small compared to the distance to the noise sources, it is assumed that all the substrate nodes are reached by an identical waveform with different phases. Suppose there exist M nodes each of them connected to a noise generator $G_m(t - \tau_m, \mathbf{\Pi}_m)$ with $m = 1, .., M$ where τ_m is the propagation delay of the waveform from one node to the other. Due to the highly non-linear dependence of performance on phase, an additive linearization around a nominal value could inaccurately model the parasitic effects of substrate. For simplicity of notation but without any loss of generality, consider only a single performance function K. The problem can be effectively addressed by deriving a worst-case sensitivity of K with respect to all parameters for which a linear behavior is observed. Let us split vector $\mathbf{\Pi}$ in two sub-vectors: $\mathbf{\Pi}'$, $\mathbf{\Pi}''$, which contain all the parasitics that show a linear and a non-linear behavior respectively. $\mathbf{\Pi}'$ is defined as the vector of all parameters such that:

$$\left|(\mathbf{S}_{\mathbf{\Pi}'}^{K})^T \cdot \triangle\mathbf{\Pi}' - \triangle K\right| < \epsilon, \tag{4}$$

with $0 < \triangle\mathbf{\Pi}' < \delta$, for some $\epsilon, \delta > 0$.
The problem of finding a worst-case sensitivity $\overline{\mathbf{S}}_{\mathbf{\Pi}'}^{K}$ is equivalent to solving the optimization problem:

$$\begin{array}{ll} maximize & \mathbf{S}_{\mathbf{\Pi}'}^{K} \\ such\ that & \mathbf{\Pi}'' \in \mathcal{R} \end{array}$$

where $\mathcal{R}$ is the feasibility region of $\mathbf{\Pi}''$. Hence, the total linearized worst-case variation of K, due to node n, can be derived as:

$$\triangle K|_n = (\overline{\mathbf{S}}_{\mathbf{\Pi}'_n}^{K})^T \cdot \triangle\mathbf{\Pi}'_n. \tag{5}$$

The introduction of worst-case sensitivity allows to reduce the parameter space and to include non-linear behavior in a certain range of performance. The local noise generator approach has three main advantages:

1. the effect of the substrate noise can be evaluated locally without taking into consideration the substrate configuration or the actual position of the devices which are injecting noise into it: the local noise generator can be seen as an antenna.

2. A standard sensitivity analysis can be used to analyze the effects of noise on performance. Furthermore, constraints on the various parameters of noise can be generated and accounted for during synthesis.
3. Once the substrate has been extracted the local substrate potential V_0 can be related to the noise generator substrate potential through an *isolation factor* α. From this value information on the placement of the analog part with respect to the digital part in the mixed-signal chip can be derived and eventually the necessity of guard rings can be pointed out.

To illustrate our approach, a model of the PLL, including a complete description of substrate noise, has been derived. Consider the VCO section of the circuit. Let $\mathbf{K} = [K_1, K_2]$ where K_1 is the oscillation period of the circuit and K_2 is the peak-to-peak jitter. The sensitivities of period K_1 with respect to all circuit parasitics have been calculated using the method of finite differences by augmentation of the schematic. A constrained optimization-based algorithm has been used to derive constraints on the parasitics [9]. Each node connected to ground through the substrate, is associated with a different local noise generator. As an example two ways of noise injection from the substrate are shown in Figure 2: the first is through the variation of MOSFETs threshold voltage (V_a and V_d), and the second is through a parasitic capacitive coupling (V_b and V_c). Let $G_n(t, \mathbf{\Pi}_n)$ be the local noise generator associated with node n. Simulations showed that the worst case happens when an impulsive function is used. Assume that we have M substrate nodes, then there exist M delayed generators $G_{n_i}(t - \tau_i, \mathbf{\Pi})\ for\ i = 1, 2, \cdots, M$. Based on the previous maximization problem, there exists a vector $\tau = [\tau_1, \tau_2, \cdots, \tau_M]$ such that $\triangle\mathbf{K}$ is maximum. Inside the VCO delay cell the worst case corresponds to having all the generators injecting synchronously with the switching of the cell itself. Under these circumstances, the sensitivity with respect to local substrate potential V_0 is about constant within the interval of interest. Considering the whole ring oscillator, the maximum degradation of the peak-to-peak jitter occurs when the delay between local noise generators is equal to the delay of the basic cell. Using the same approach as for the VCO, sensitivities of the loop filter and of the charge pump were evaluated. The values of sensitivity resulted to be much less than the one of the VCO. Thus no constraints need to be generated for these two components.

4 Substrate Noise Characterization

Modeling transmission of noise through substrate is quite complex and computationally intensive. With typical substrate doping levels, used in commercial processes, the substrate impedance is mainly resistive up to $3 - 5\ GHz$ [4]. Several attempts have been made to address the problem efficiently, either extracting the complete resistive mesh [11] or approximating the substrate with analytical models [10]. In this work we use SubRes, a package for efficient substrate analysis based on the use of the Green Function [4]. For each contact on the surface, resistances to every other contact and to the backplate are evaluated (see Figure 3). Hence, a square matrix of dimensions equal to the number of contacts being analyzed is generated.

Once constraints are generated on local noise generators and a complete characterization of the transport through the substrate is carried out, we turn our attention to noise sources. Substrate noise is injected mainly through devices and capacitive coupling from interconnects. During each transition, digital CMOS gates inject spurious currents into substrate by virtue of mechanisms of impact ionization and drain/source-substrate junctions. But, while junction injections

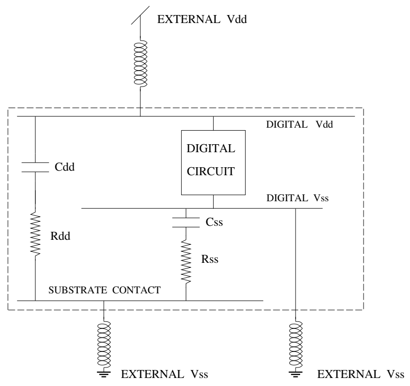

Figure 4: Schematic representation for circuit simulation of dividers.

are easily modeled through discrete capacitances, the impact ionization phenomenon needs to be analyzed more in depth.

Electron-hole pairs are generated in the pinch-off region, when the electric field exceeds approximately the critical value of $4 \cdot 10^4\ V/cm$; in the case of an nMOSFET, the added electrons contribute to an increased drain current, while the holes constitute a substrate current. The total current produced by impact ionization can be expressed through the following equation:

$$I_{impact} = \frac{A}{B} l E_m I_d e^{-B/E_m} = C_1 (V_{ds} - V_{dsat}) I_d e^{-\frac{C_2}{(V_{ds} - V_{dsat})}},$$

where V_{ds} is the drain-source voltage and V_{dsat} the saturation voltage [12]. To determine parameters C_1 and C_2 the device simulator Pisces [13] has been used. These parameters have then be utilized in standard Spice models.

Impact ionization induced current is caused by hole injection, therefore it can only be positive. This means that during both transitions High-to-Low and Low-to-High of a digital gate, we have a positive pulse of current injected in the substrate. Hence we have low frequencies and DC components in the spectrum of the signal injected in the substrate. On the contrary injection due to capacitive coupling provides positive and negative contributions according to the direction of the transition.

There exist two main types of substrates: one referred to as *low-resistivity substrate* which consists of a thick, high-resistivity epitaxial layer (thickness d $\simeq 10\mu m$, resistivity coefficient $\rho \simeq 10 \div 15\ \Omega cm$) and a low-resistivity bulk($\rho \simeq 1 m\Omega\ cm$). A second type, referred to as *high-resistivity substrate*, is composed of a uniformly doped layer with $\rho \simeq 20 \div 50\ \Omega cm$. Recently the low-resistivity substrate with a high resistivity epitaxial layer has been widely adopted for its latch-up suppression properties [12].

If we consider a very large digital circuit with hundreds of thousands of transistors a complete substrate extraction is infeasible. The possibility of reducing such a circuit into clusters which share the same *injection characteristics* would be highly desirable. It has been shown in [4] that in case of low-resistivity substrates the relative location of different parts of the circuit is not critic within certain spatial limits. Based on this assumption we propose a partitioning based on time rather than on space. In a digital circuit typically we have the biggest number of transitions happening simultaneously with the clock and then a certain number of others following in cascade in the combinational blocks among registers.

We propose to model as a single *equivalent noise source* injecting through a single contact of appropriate dimensions and location, to be determined with SubRes, all the gates switching together within a certain area. In this way the injection activity of the whole chip can

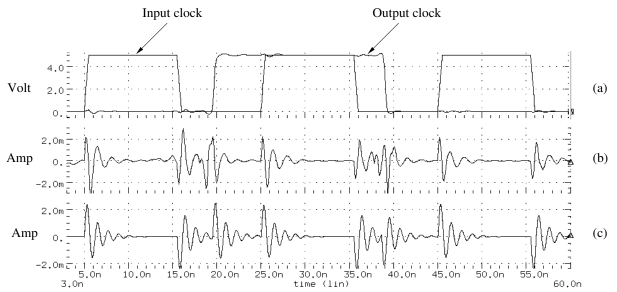

Figure 5: (a) Divider's input/output waveforms; (b) Noise injected in the substrate obtained by SPICE simulations; (c) Model derived for the *equivalent current source*.

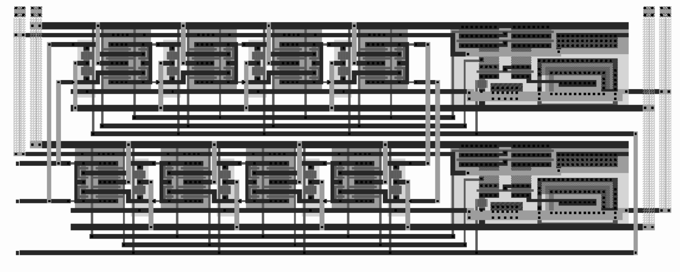

Figure 6: Layout of the VCO generated by VCOGEN.

Performance	Ideal Value	max degradation
oscillation period	$10 - 20ns$	10 %
peak-to-peak jitter	0	$100ps$

Table 2: Design specifications of the VCO.

be represented by few hundreds of equivalent noise sources which can be easily extracted by SUBRES and simulated with SPICE to evaluate the cumulative effect on the analog part of the circuit. In this approach clock skew needs to be taken into account. Clock skew, if properly controlled, can be used to reduce the effect of the switching activity. In fact, if performing the proposed substrate-aware sensitivity analysis we realize that the analog circuit is more sensitive to the peak value of the substrate noise rather than to its duration in time, we can introduce some delay elements to generate clock skew. Using this strategy, as long as the correct functionality is preserved, the peak value of the current injection can be significantly reduced.

In the PLL test case the most important sources of switching noise are the three dividers illustrated in Figure 1. Simulations with SPICE have been performed of the dividers extracted from their layouts. The schematic illustrated in Figure 4 has been used to take into account all the parasitics not automatically extracted like parasitic inductors due to bonding wires. From the results of these simulations it can be pointed out that the whole switching activity is concentrated around two main events: fall and rise of the input clock and fall and rise of the generated clock. In Figure 5(a,b) results of SPICE simulations performed on one of the extracted divider are shown and in Figure 5(c) the model derived for the two current sources to be used to represent the switching activity in the evaluation of the total noise sensed by the analog circuit is depicted.

The enforcement of substrate-related constraints is performed in the following way. First a technology-aware model of the substrate for the entire chip is built. Then, given that the signal injected by each noise source is known, the isolation factor α required to meet the derived constraint on the V_0 is calculated. Finally SUBRES is used to drive a placement tool towards a configuration where all specifications are met.

5 Results

A VCO module generator, VCOGEN, has been realized and the constraints on the substrate noise have been used to place the VCO inside a PLL. The placement tool PUPPY-A [14] has been modified to account for the substrate model.

An appropriate floorplan for the VCO was chosen to account for various considerations. First, critical capacitive and resistive parasitics could be easily minimized by abutting all delay elements of the ring oscillator. Second, full scalability, both in power and frequency was allowed. Third, due to multiple folding of the ring oscillator's structure, technological mismatches could be contained. In addition, by keeping the cell's aspect-ratio low, the systematic component of the mismatch relevant to the circuit could be reduced to one dimension as suggested in [15]. The fully differential implementation of the VCO can acquire a better isolation to substrate noise capacitively coupling through interconnections with respect to a single-ended one. The delay element and the distributed bias of the VCO are depicted in Figure 2. The layout of the delay element has been designed using a mirror symmetry. This configuration has two main benefits:

1. a minimization of rising and falling time mismatch;
2. the effect of thermal and substrate noise is minimized due to the balance of the two branches.

An 8-stage VCO for a PLL has been automatically synthesized using module generator VCOGEN (see Figure 6) in a CMOS $1\mu m$ technology. The relative position of the VCO with respect to the dividers, the main source of substrate noise, has been enforced using substrate resistance estimations performed by SUBRES . Table 2 illustrates the maximum

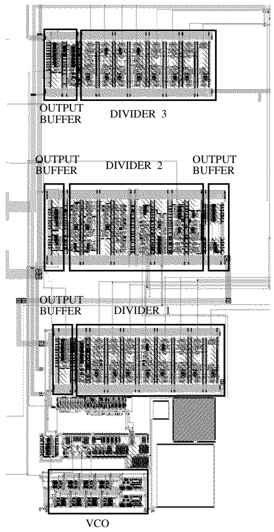

Figure 7: Layout of the entire PLL.

performance degradations to be enforced. The PLL layout has been partitioned in clusters according to the switching time as described in Section 4. In Figure 7 eight clusters are highlighted. The areas named *divider* are synchronous with the input clock of the divider

Parasitic	Constraint	Extracted value
C_{out+}	$12.34fF$	$11.60fF$
C_{out-}	$12.34fF$	$11.60fF$
C_x	$15.84fF$	$1.12fF$
$V_0\|_{VCO}$	$120mV$	$108mV$

Table 3: Constraints obtained by the sensitivity analysis compared with the extracted values.

Variable	size with parasitics	size without parasitics
W_p	$36\mu m$	$25\mu m$
L_p	$1\mu m$	$1\mu m$
W_n	$2.6\mu m$	$2.6\mu m$
L_n	$4\mu m$	$4.6\mu m$

Table 4: Transistor sizes obtained by the circuit optimization.

Operation	CPU time (sec)
circuit optimization	1028 †
substrate sensitivity	2545 †
interconnect sensitivity	3256 †
constraint generation	115
layout generation	43

Table 5: results obtained on a DECstation 5000/125 and on a DECstation alpha (†).

while the ones named *output buffer* are synchronous with the clock generated by the divider itself. A contact of size equal to the total injecting area(i.e. devices, interconnects, etc.) has been assigned to each cluster. Then the extraction of the substrate resistances connecting these contacts to the one associated to the VCO have been performed through SUBRES. Finally, SPICE simulations have been carried out using as current sources the models shown in Figure 5(c). The result of these simulations, shown in Figure 8, is the estimate of the noise sensed at the VCO substrate end. The specification on the peak-to-peak jitter induced by substrate noise represents the worst-case scenario. In this scenario the noise signal reach the VCO during a transition of each delay element. In this case, however, the divider is triggered by the VCO. Thus the digital switching activity due to the dividers happens always with a certain delay with respect to the VCO switching giving a bigger safety margin.

The sensitivity analysis of interconnect in the VCO has been performed introducing 16 parasitics per cell. The constraints on critical parasitics are summarized in Table 3. Table 4 shows the transistor sizes

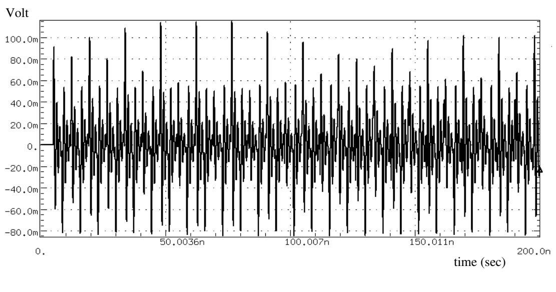

Figure 8: Substrate noise sensed at the contact associated with the VCO.

obtained from the optimization with and without taking into account parasitic analysis. It can be seen as in the first case the dimensions are bigger to reduce the sensitivity, as described in Section 2. Finally Table 5 shows all the CPU times needed to run the tools being used.

6 Conclusions

A new methodology has been presented which accounts for substrate noise coupling at each level of the top-down constraint-driven design. Modeling of layout parasitic effects and sensitivity analysis have been proposed as an effective aid for the design and optimization of a class of mixed-signal circuits. A more realistic optimization can be achieved and the dependence of performance from second-order effects can be contained within pre-defined bounds. Use of performance sensitivities has been extended to derive a set of constraints on the substrate noise locally. Hence, substrate extraction is necessary only during placement and verification. By enforcing the constraints, the high-level specifications are guaranteed to be met. A test case of a PLL realized with a $1\mu m$ CMOS technology has been fully implemented using semi-automated constraint-driven layout synthesis.

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