A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology

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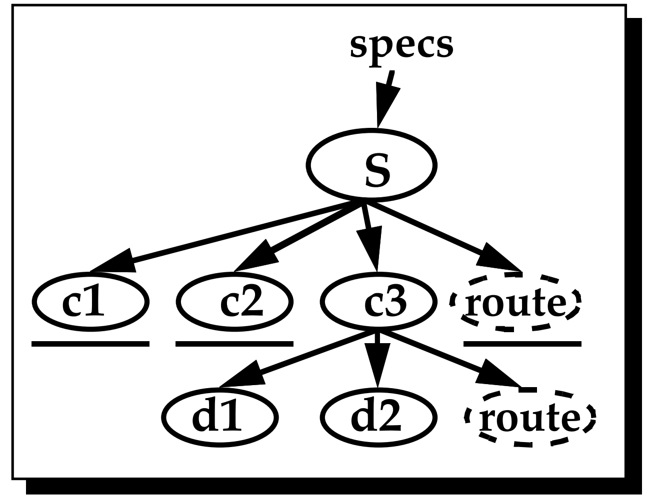
Motivation

- **Analog circuitry is often the bottleneck of large mixed-signal systems**
  - **non systematic, more intuitive**
  - **time consuming**
- **We have proposed top-down design methodology**
  - **hierarchical approach** *(Chang et. al. CICC '92)*
  - **provide rigorous tools at every level of hierarchy**
  - **help analog designer, not substitute**
- **To prove the suitability of the methodology we need:**
  - **efficient tools to handle complex mixed-signal designs**
  - **industrial strength, fabricated design examples (Real systems !)**

Outline

- Motivation
- ☛ Background on Top-Down Design Methodology
- Methodology for Video Driver Design
  - PLL High Level Design
  - Circuit Level Design
  - Layout
- Experimental Results
- Summary - Future work

Key points of the Methodology



- Start with a system and constraints
- Choose architecture of components
  - High level simulation
- Propagate constraints from current to next
  - Behavioral Simulation
  - Optimization
- Repeat process until done
  - library component, module generator, transistor level design
- Constraint -driven physical synthesis
- Verify design bottom-up
  - Extraction
  - Hierarchical simulation

Advantages

- Systematic hierarchical approach
  - Efficient exploration of design space
  - Early verification (behavioral simulation)
  - Guaranteed feasibility
- Reduces overdesign
- Less design iterations
- Fast verification (bottom-up)

Faster time-to-market

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Video Driver System

- Large commercial system (PC, workstation monitors)
- Includes PLL
  - many applications
  - hard design problem
  - models and tools needed
  - novelty: use beh. simulation to propagate jitter constraint

Performance

range: 25MHz - 135MHz

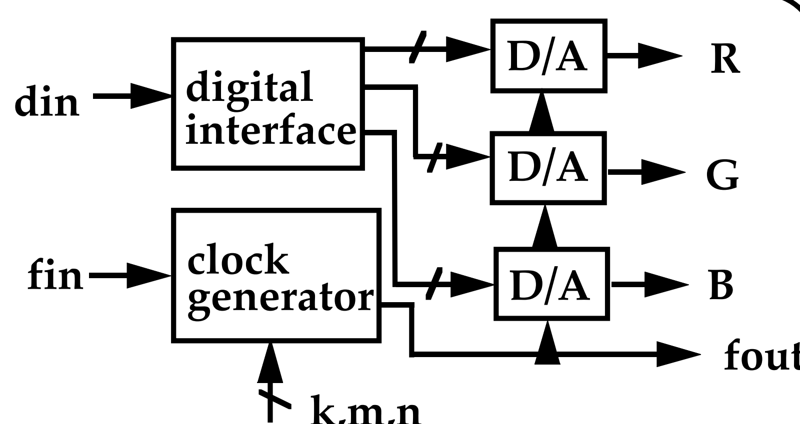
resolution: 8 bits

timing jitter < 1 % rms

Supply: 5V

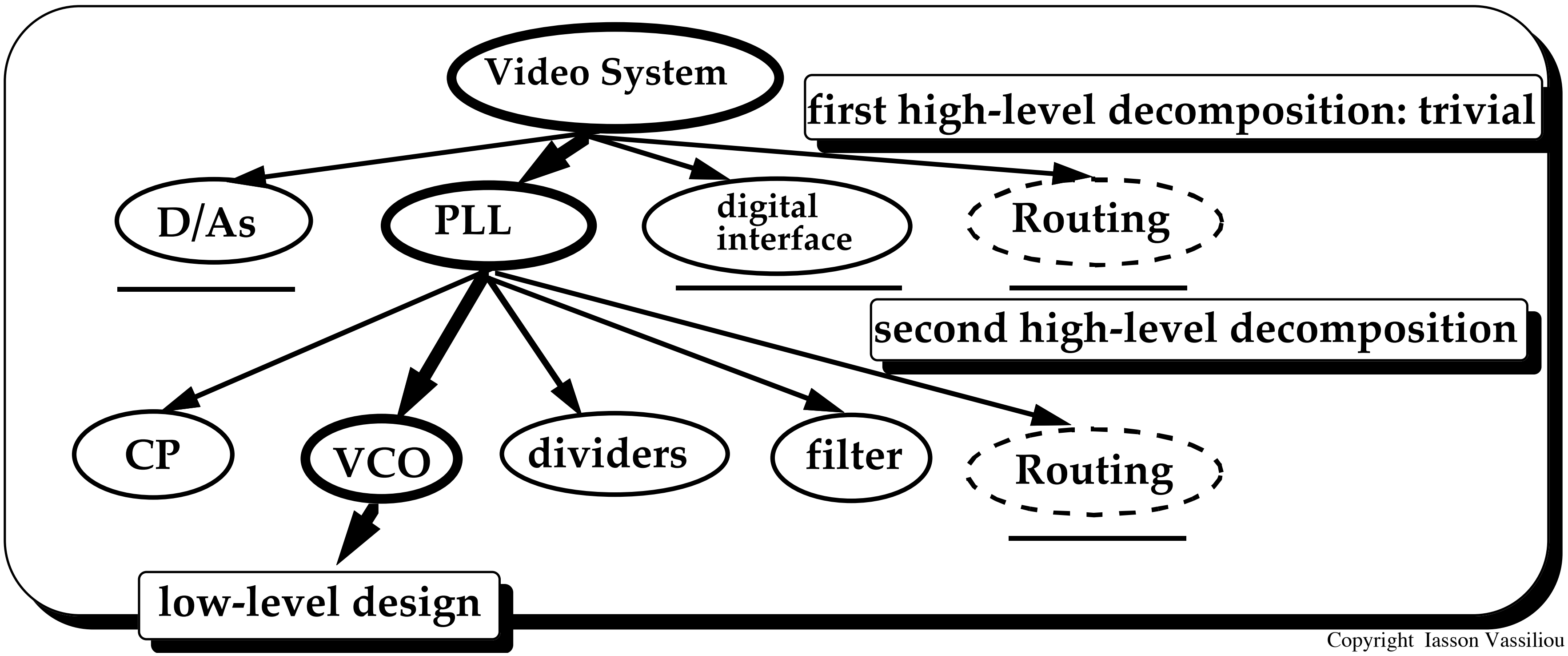
Technology: MOSIS HP 1.0u

Power: minimize



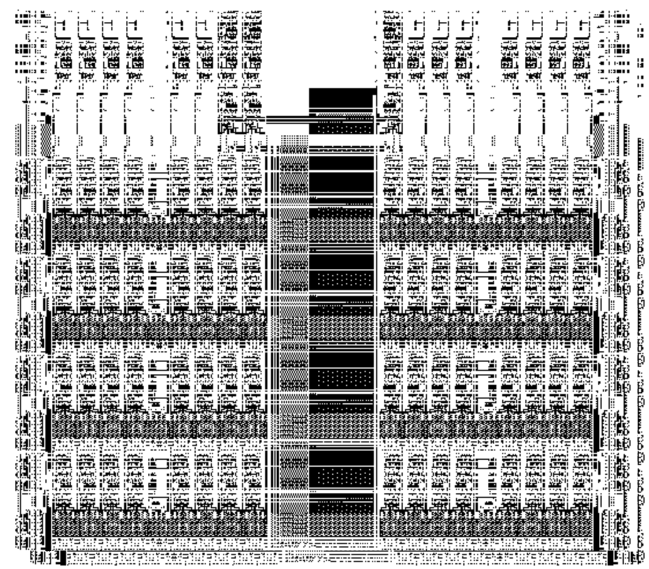
High Level Decomposition

- For the D/As module generators are used
- PLL clock generator: follow methodology to layout



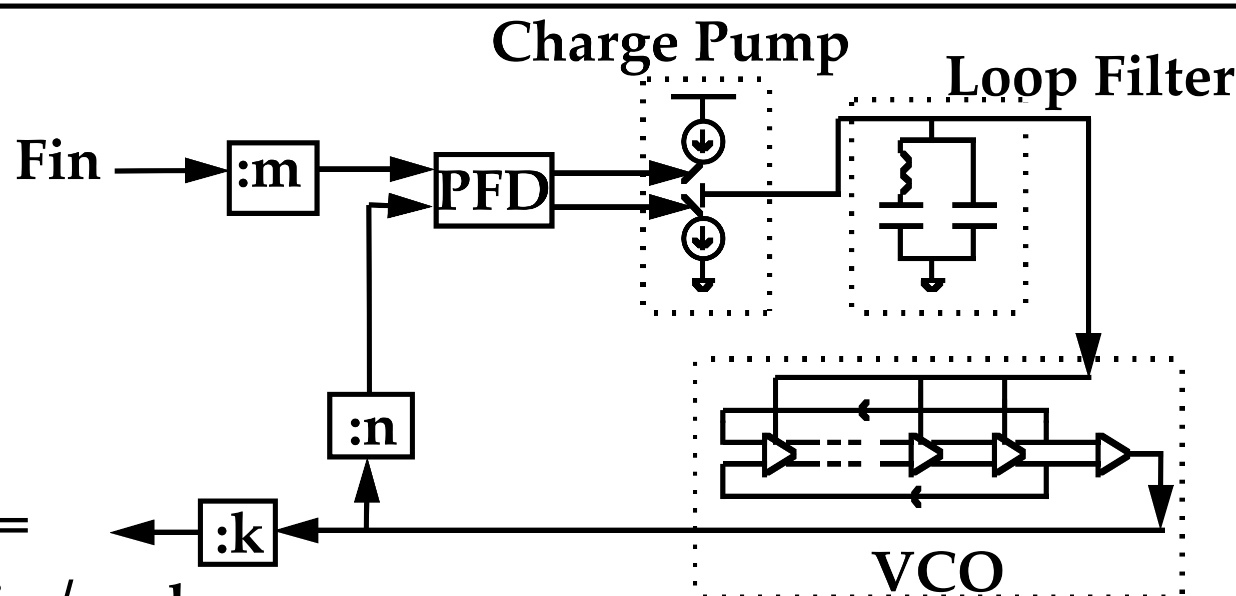
Video Driver System
D/A converter synthesis

- Specifications
  - resolution: 8 bits
  - INL, DNL: 1LSB
  - speed: 150MHz
- Use module generator for current source, interpolative D/A
  - ~1.5 CPU hours on DEC alpha



R. Neff et al CICC '95

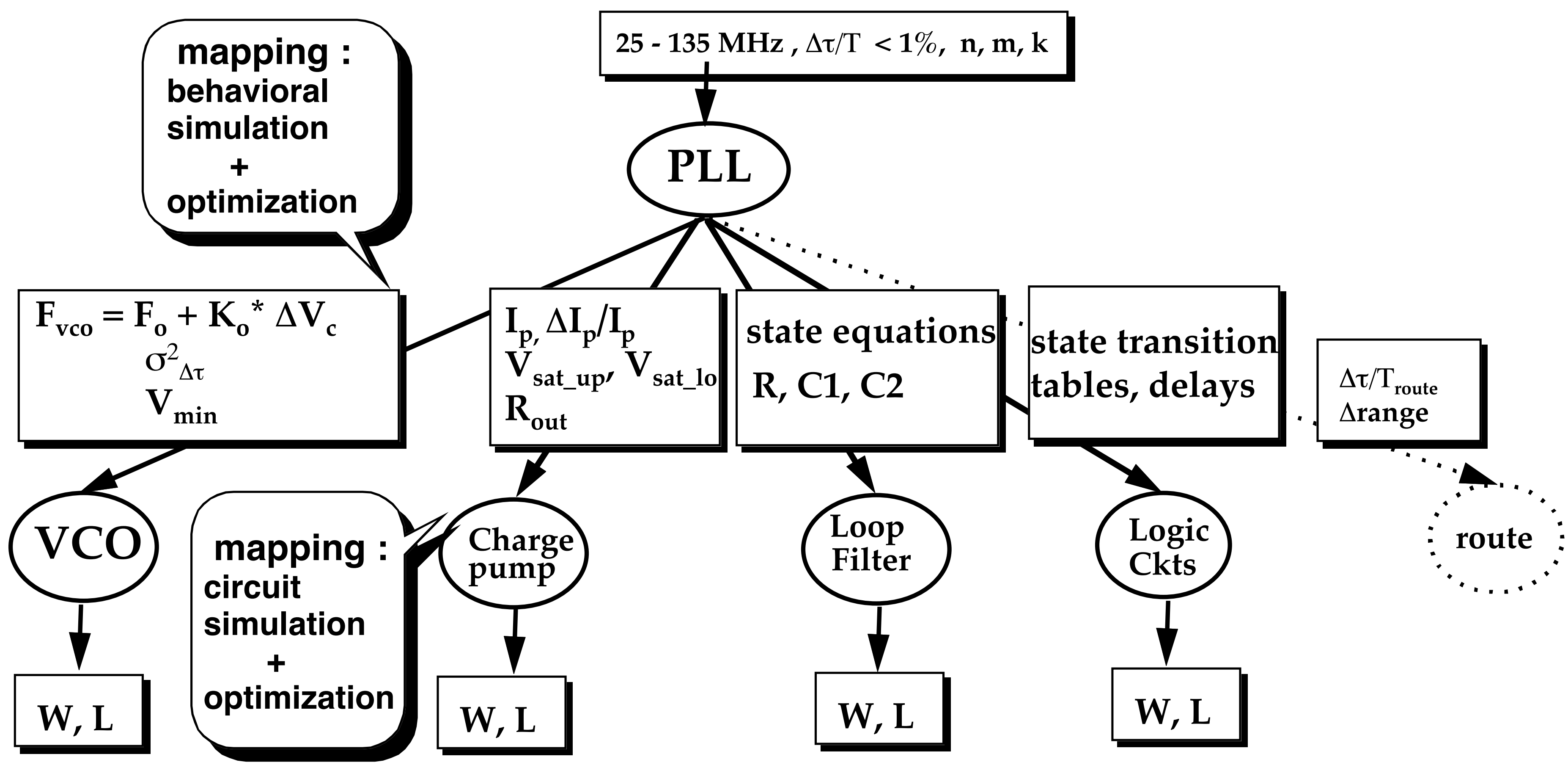
Architecture Selected: PLL



Fout = n x Fin / mxk

- Charge-Pump PLL with ring oscillator VCO
- Fixed F_{ref}, m, n, k to produce given frequencies

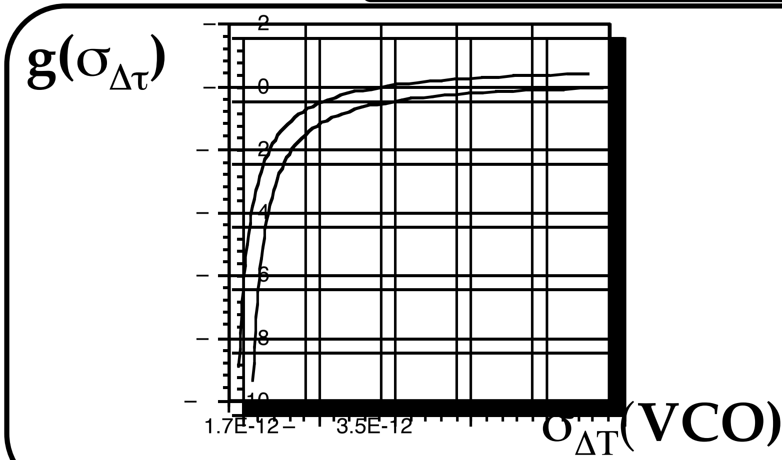
Hierarchical Decomposition/Mapping: PLL

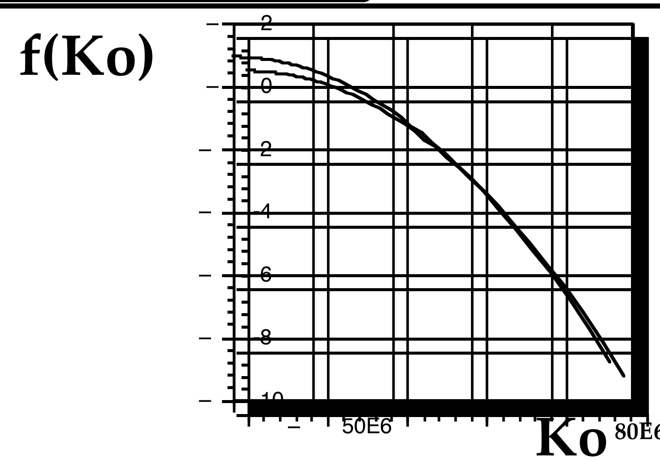


High Level Optimization - 0bjective

- flexibility(Ko , $\sigma^2_{\Delta\tau}$, R , C , Ip) = f(Ko) + g($\sigma^2_{\Delta\tau}$) + h(R) + i(C) + j(Ip) + ...
- Flexibility functions based on
  - design experience
  - circuit equations

Example flexibility functions:





High Level Optimization - Problem Formulation

$$
\begin{array}{lll}
\max & \text{flexibility}(R, C, C_1, I_p, K_O, \ldots) & \\
s.t. & T_{acq} \leq T_{max} & \\
 & PM_{PLL} \geq 45^{O} & \\
 & \Delta T / T_{fmax} \leq 0.7\,\% & \\
 & R_L \leq R \leq R_U & \\
 & \vdots & \\
 & K_{OL} \leq K_O \leq K_{OU} &
\end{array}
$$

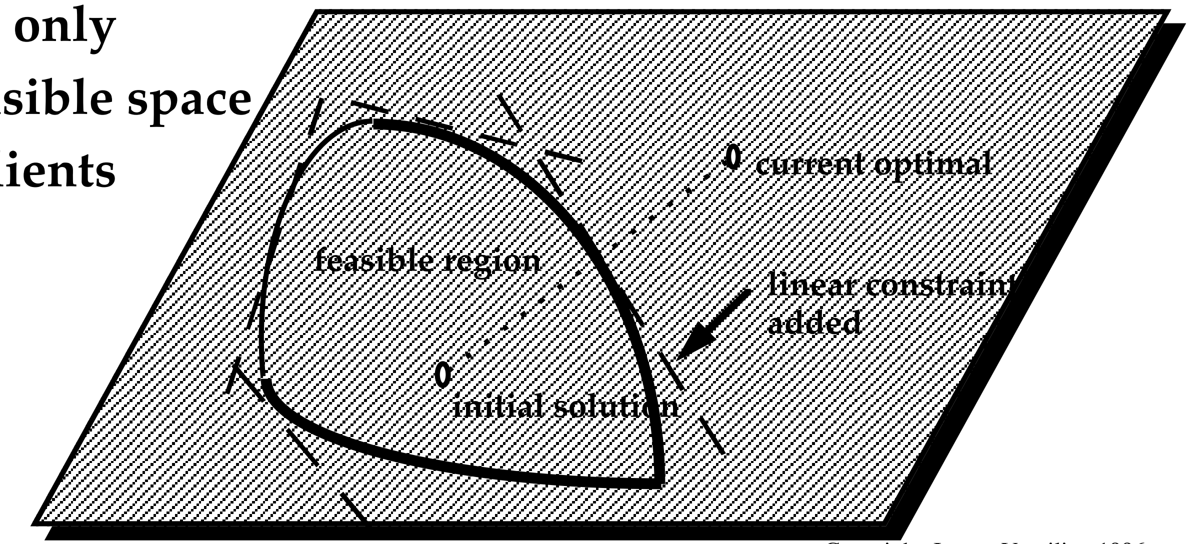
Constants

Fo	**100 MHz**
V_{sat_up}	**4.8 V**
V_{sat_lo}	**0.2 V**
$\Delta I_p/I_p$	**5 %**
R_{out}	**2 MΩ**
V_{min}	**1.8 V**
ΔR, ΔC	**20%**
ΔK	**50%**
ΔFo	**30%**

- **Jitter simulation**
  - **Check worst cases for stability**
  - **Computes jitter if stable**
  - **Uses behavioral simulation techniques**
- **Phase margin > 45^{O} : parameter variations**
  - **Computed analytically**

High Level Optimization - Algorithm

- Most non-linear optimization algorithms require accurate calculation of derivatives
- Timing jitter from Monte-Carlo Simulation - inaccurate derivatives
- Method used: Supporting Hyperplane
  - requires 1st derivative only
  - derivatives only in feasible space
  - works with noisy gradients
  - requires convexity
  - provide initial point



High Level Optimization - Algorithm (cont.)

- Initial point: given
- Derivatives:
  - finite differences
  - iteration to find stepsize (noisy gradients)
  - inside feasible region
- Compute “cheap” constraints first
  - if not satisfied no need to compute expensive ones
- Non-convexity
  - reduce variables by 1
  - solve for various values of eliminated variable
- Loss of optimality ?
  - OK, objective is heuristic
  - cheap feasible solution fast

High Level Optimization - Results

objective

flexibility = 2.79

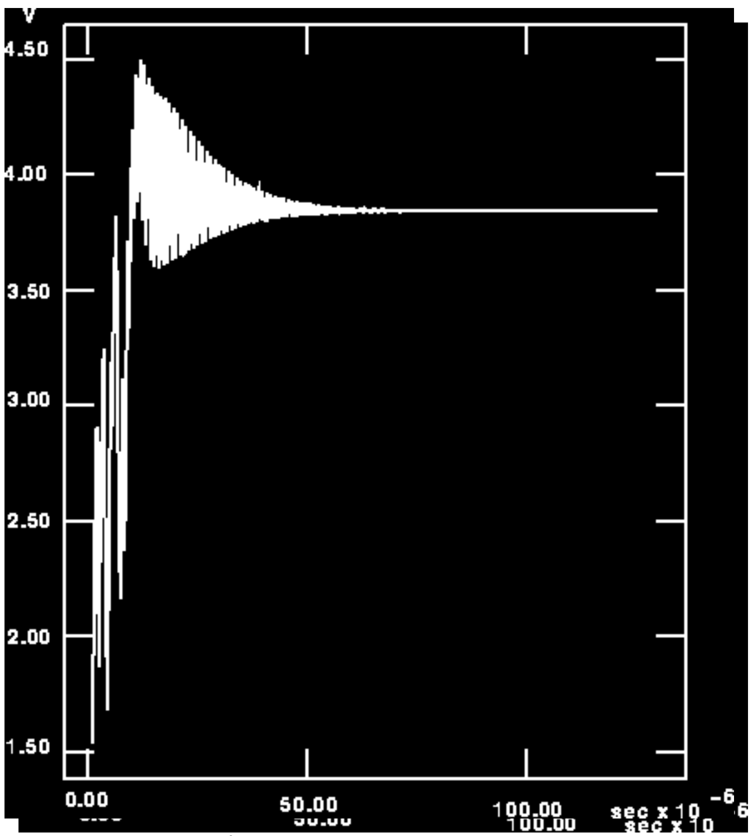
constraint	value
$jitter_{140MHz}$	0.7%
phase margin	44^{o}

Parameter	Value
R	200.5k
C	57.8pF
C1	5pF
Ip	15.8uA
$\Delta\tau_{VCO}$ (140MHz)	3.33ps
Ko	40MHz/V

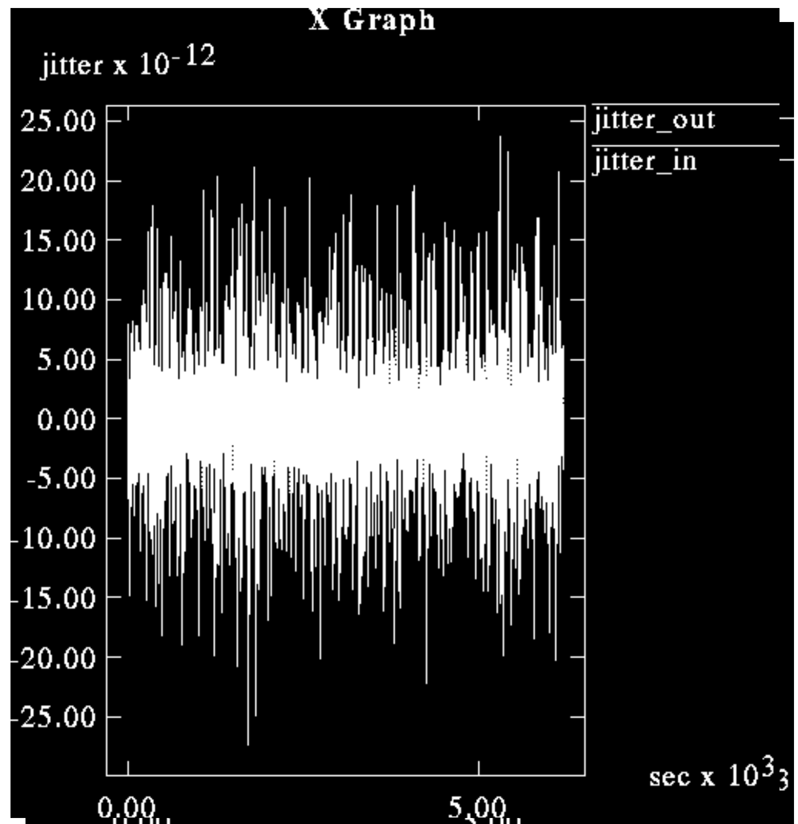
Iterations	8	
CPU	7600 sec	(DEC Alpha)

- Tolerance to parameter variations verified

High Level Optimization - Results



Transient response



Jitter simulation

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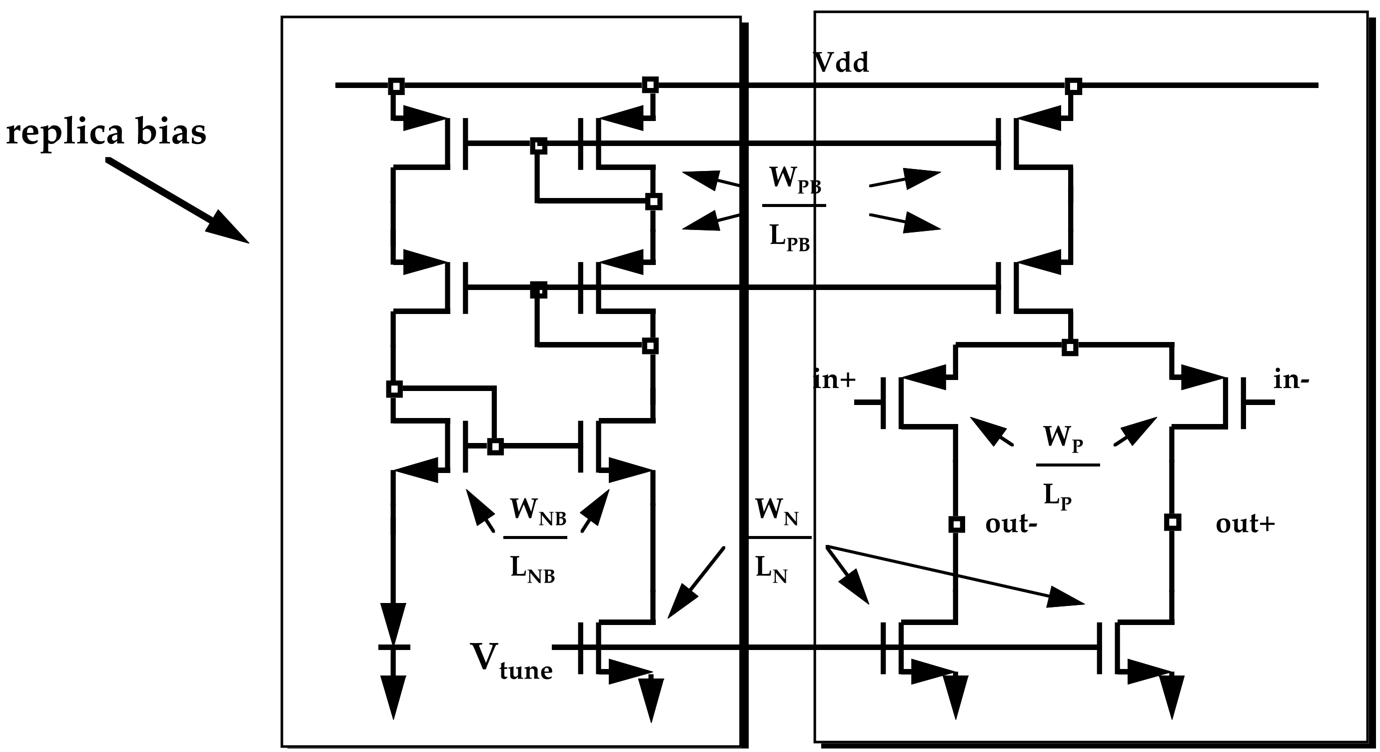
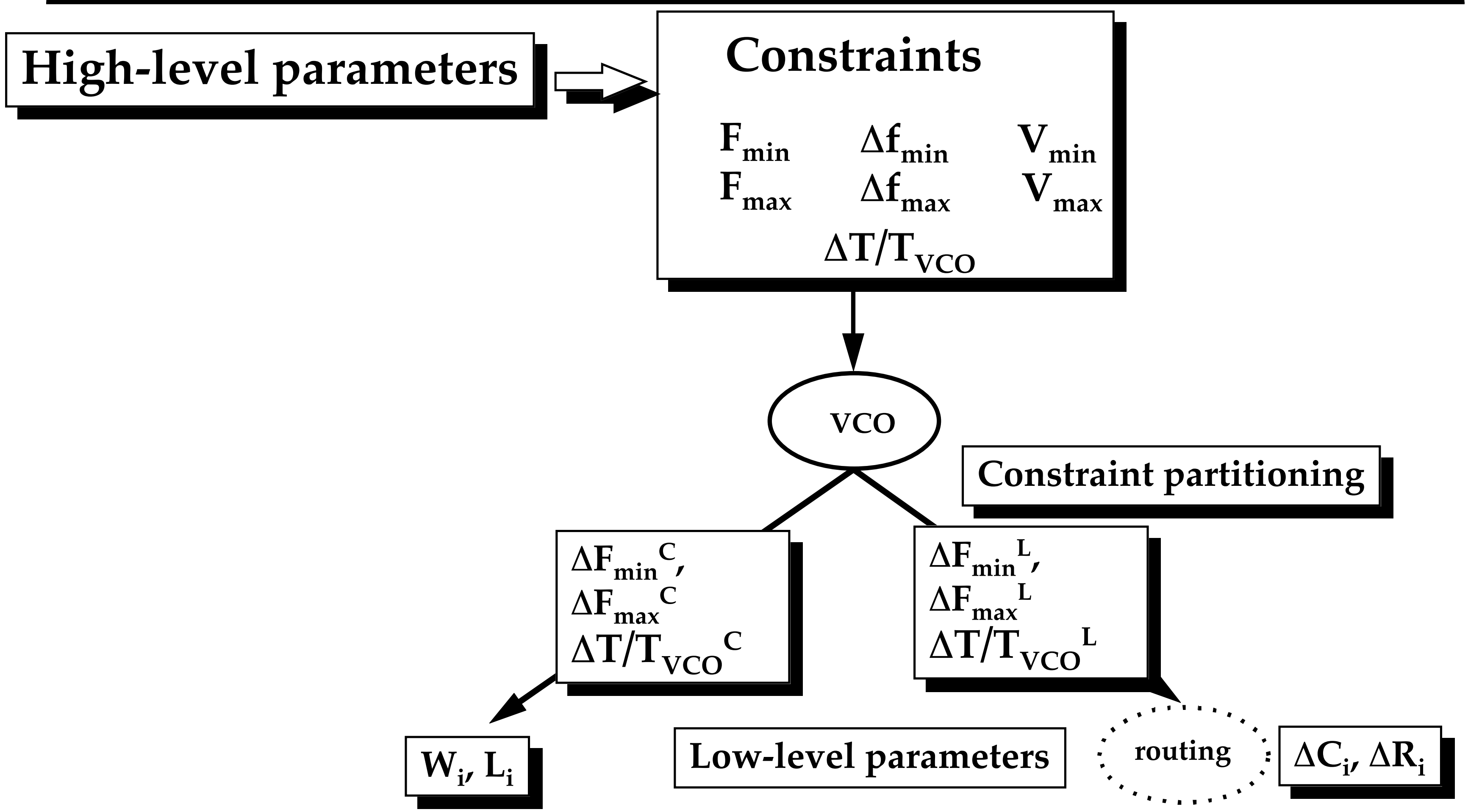
VCO Topology

- 8 stage ring oscillator VCO
- use differential cells to reject supply noise



(similar to D. Reynolds ISSCC 94)

VCO decomposition



Low Level Optimization - VCO

$$
\begin{aligned}
\min \quad & Power(Wi, Li, \ldots) \\
s.t. \quad & \Delta T_{VCO\,140\,MHz} \le 3ps \\
& F_{MAX} - \Delta F_{MAX} \le F_{MAX} \le F_{MAX} + \Delta F_{MAX} \\
& F_{MIN} - \Delta F_{MIN} \le F_{MIN} \le F_{MIN} + \Delta F_{MIN} \\
& V_{MIN} \le V_1 , \quad V_2 \le V_{MAX} \\
& \boxed{\left[S_C^P \right]^T \bullet \Delta C_{max} \le \Delta P_{max}} \\
& Wi_L \le Wi \le Wi_U , \; Li_L \le Li \le Li_U
\end{aligned}
$$

Constants

L_{nb}, L_{pb}	**1 u**
W_{pb}	**20 u**
W_{nb}	**10 u**
ΔC_{Lmax}	**50 %**
ΔC_L	**15 fF**

Key idea use sensitivities and parasitics estimate

- ✓ **Fmin, Fmax: simulation (Spice)**
- ✓ **ΔT_{VCO} : equations**
- ✓ **Algorithm : Supporting Hyperplane**

VCO Optimization - Results

Performance

- **Fmax = 163MHz**
- **Fmin = 48MHz**
- **ΔT_{rms} = 1.5 psec @140MHz**
- **Power = 6.2 mW**

Variables

- **Wn 2.6u**
- **Ln 4u**
- **Wp 36u**
- **Wp 1u**

4 Iterations

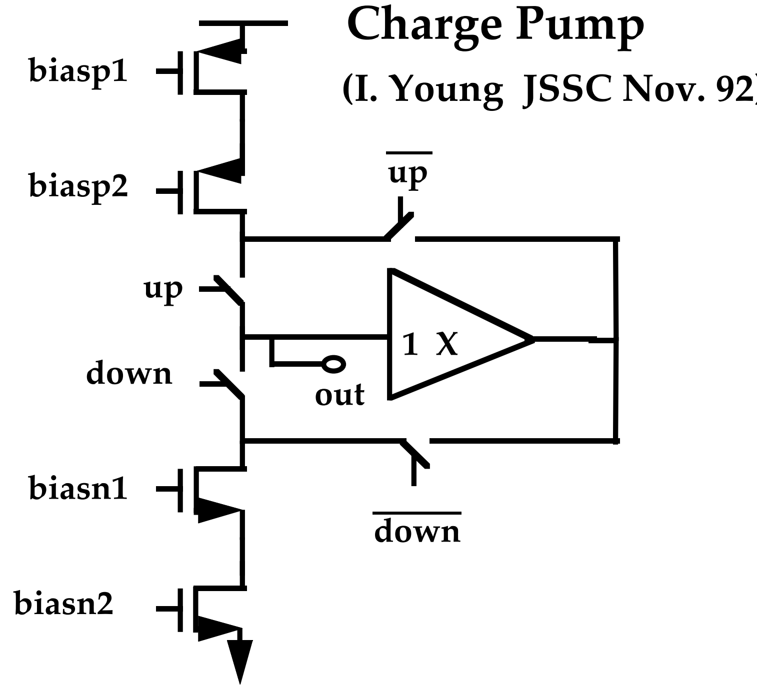
2070 CPU sec (DEC Alpha)

Low Level Decomposition

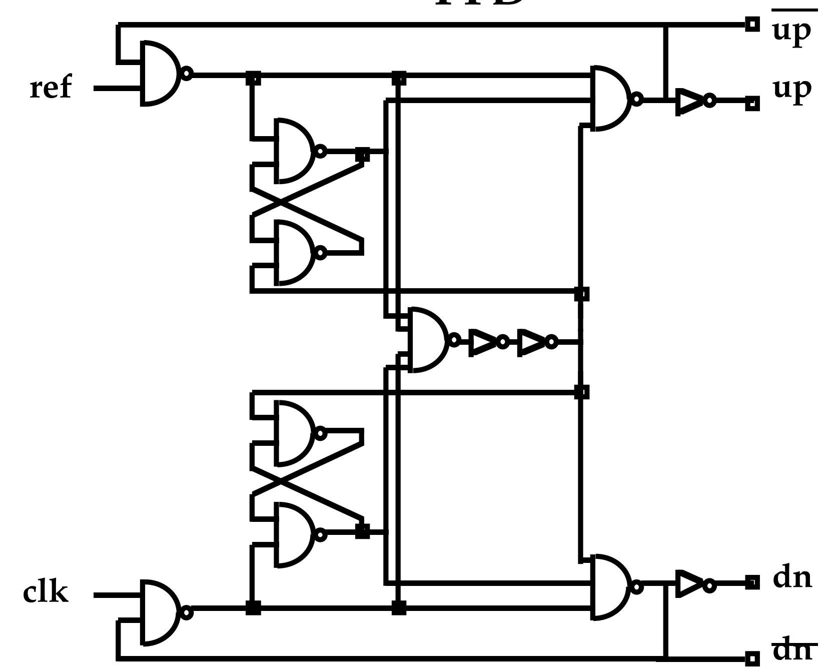
- Other cells: automatic layout generation or standard cell techniques
  - Verify performance

Charge Pump

(I. Young JSSC Nov. 92)



PFD



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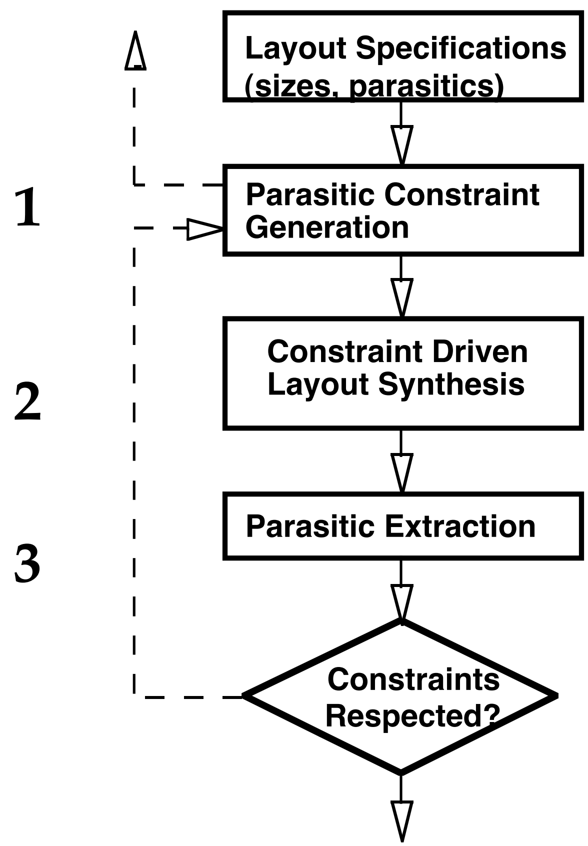
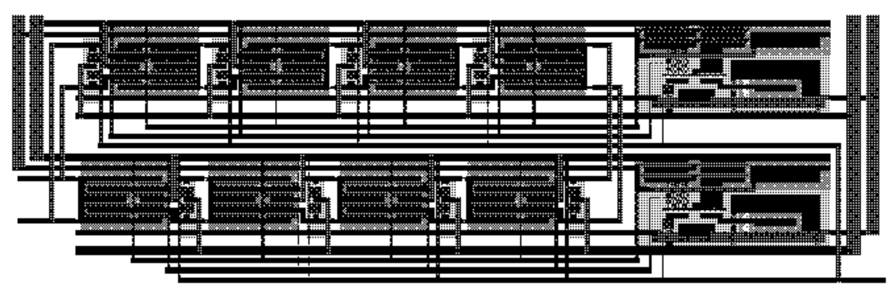
Layout Design Flow

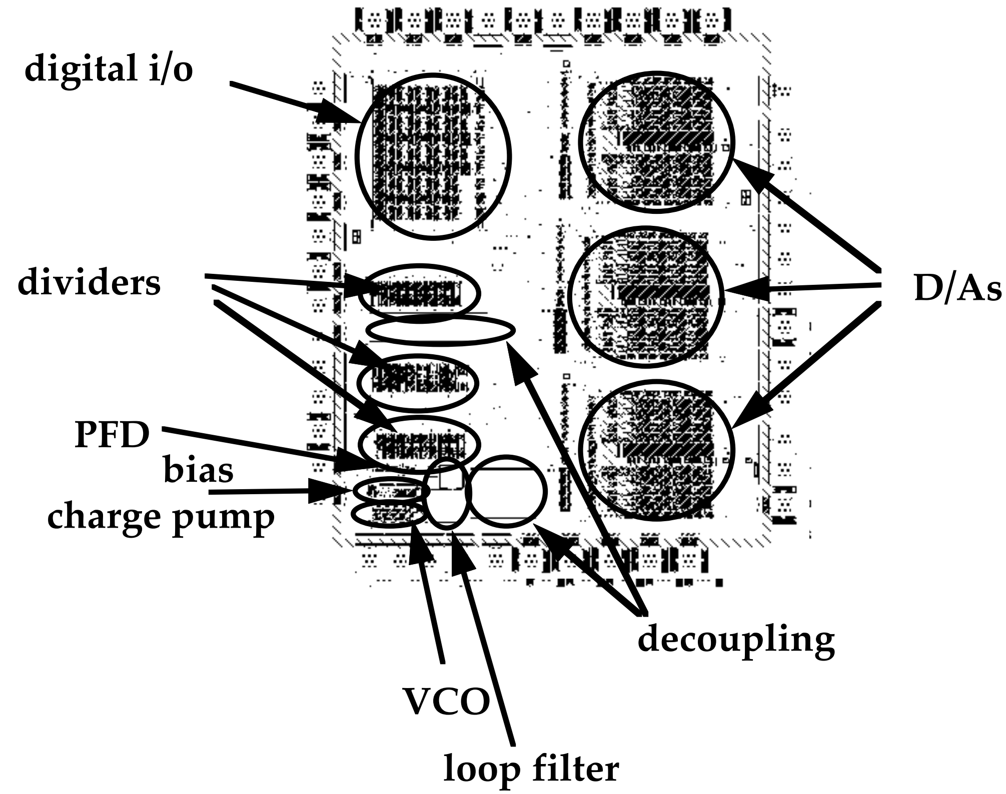


- Module Generation: VCO
  - Fully parametrized
  - All bus sizes adjustable
  - Fully scalable
  - Fixed floorplan



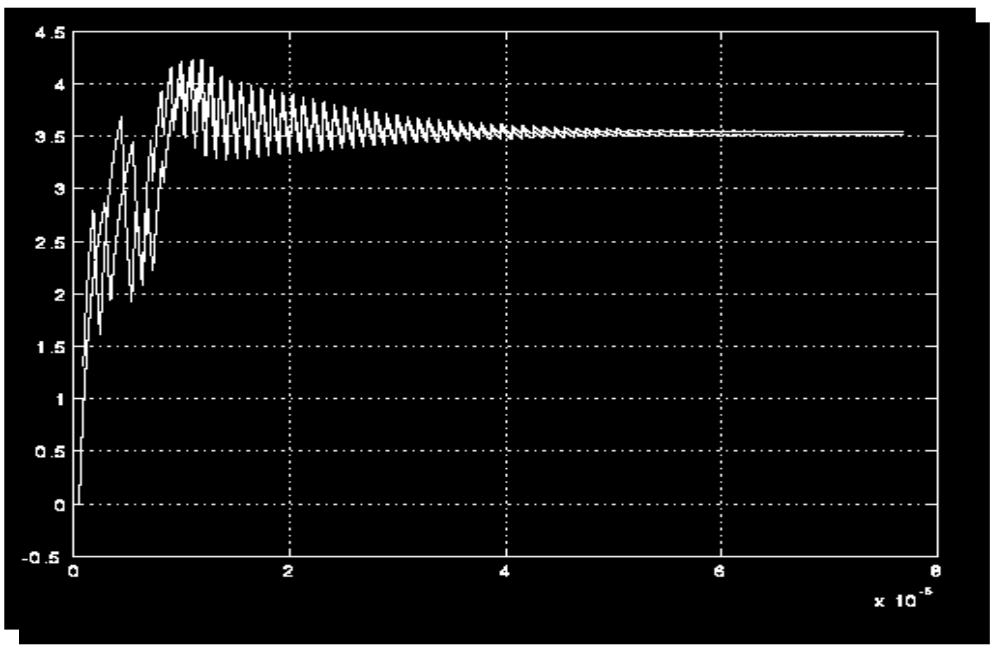
Video Driver Layout

- ~20,000 transistors
- used OCTTOOLS for automatic routing
- total area: 3.4mm x 3.9mm



Bottom-up Verification

- Bottom-up verification performed
  - individual components at circuit level (Spice)
  - PLL using behavioral simulation with extracted parameters

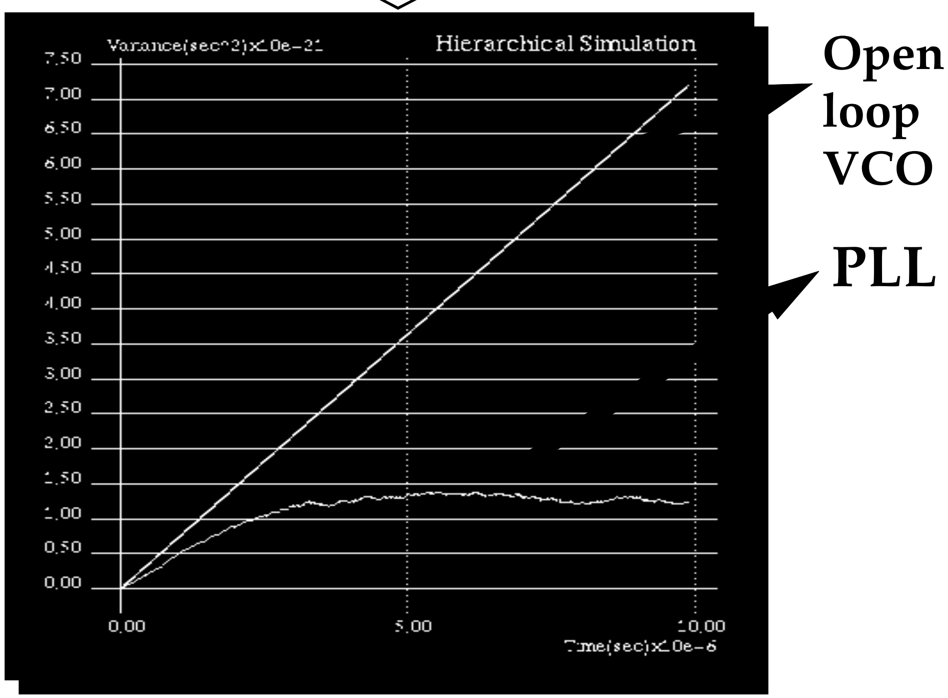


Transient Simulation

SPICE : 20 CPU hours
Behavioral : 250 CPU secs
(DEC Alpha)

Bottom-up Verification (cont.)

timing jitter variance



- Hierarchical Simulation
  - VCO: noise simulator (A. Demir et al ICCAD '94)
  - PLL: Behavioral

RMS Jitter
Simulation: 48 psec
Measurement: 65 psec

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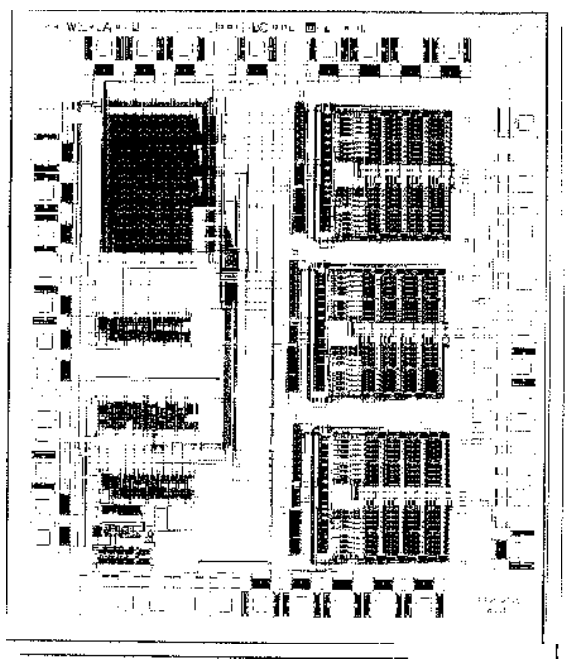
Experimental Results

Chip fabricated
(1.0u MOSIS process)



Measurements

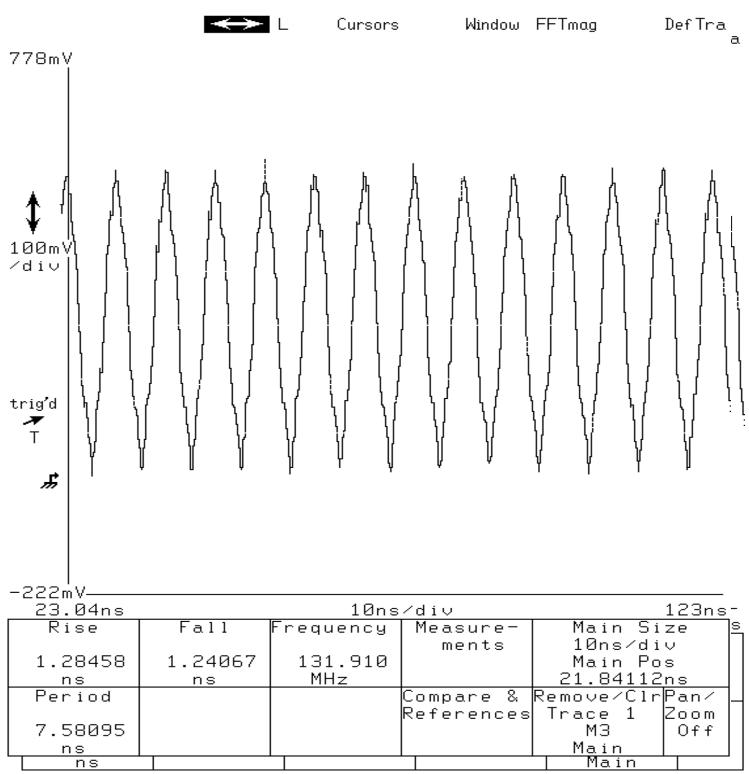
D/A

◆**INL**	**0.15 LSB**
◆**DNL**	**0.05 LSB**
◆**Settling time (2%)**	**6ns**

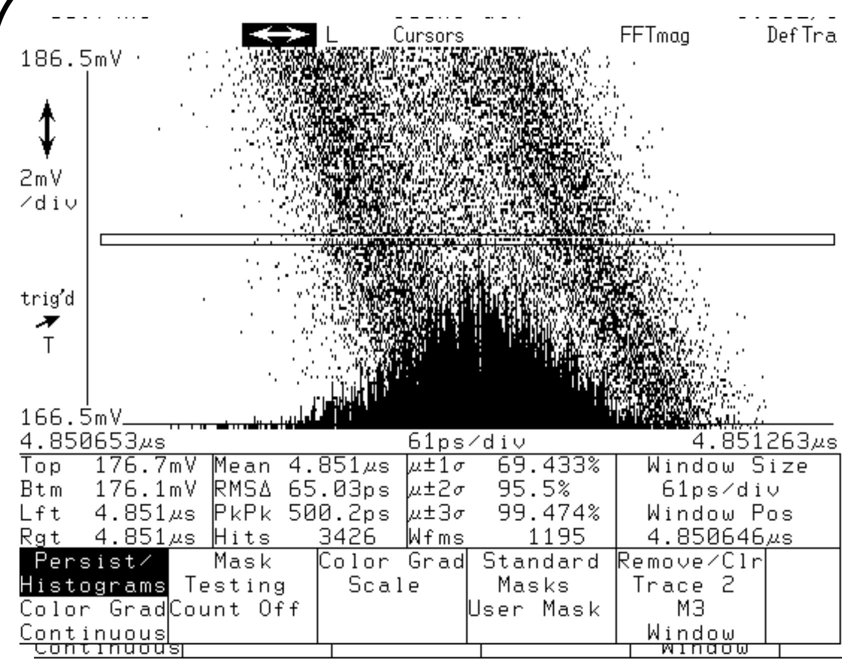
PLL

◆**Range**	**5Mz - 130 MHz**
◆**Jitter**	**0.65% @100MHz (65 ps)**

Experimental Results (cont)

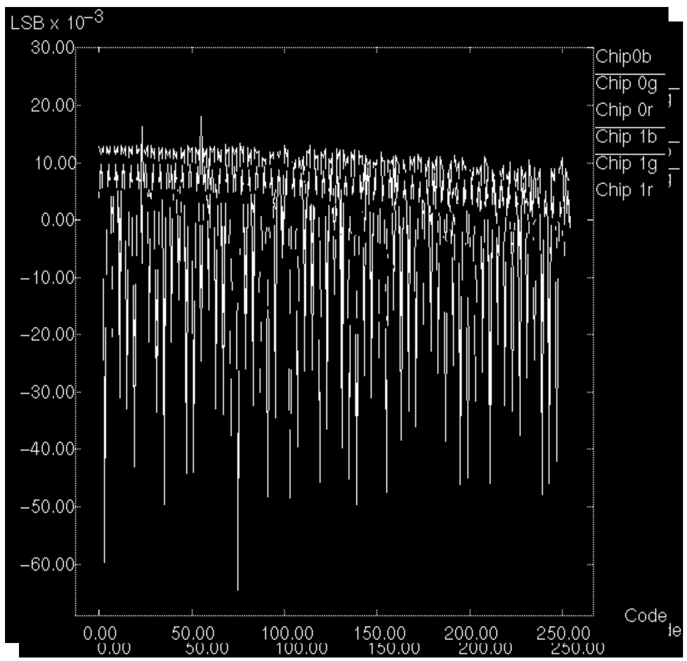


Clock output waveform

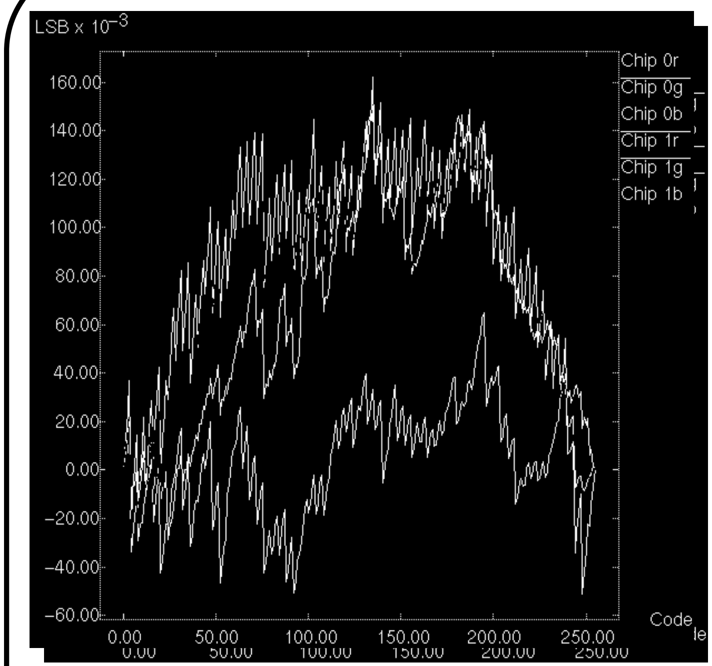


Jitter histogram

Experimental Results (cont)



D/A INL



D/A DNL

Summary - Future work

- Developed techniques to apply top-down methodology in a complex mixed-signal system
- Complete design example from specifications to working fabricated parts (first design)
  - hierarchical approach - propagate jitter constraint
  - behavioral simulation
  - optimization
  - bottom-up verification
- Apply methodology and expand use to other designs
  - RF systems