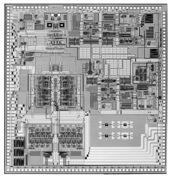
A Design Methodology for Analog Systems Based on a Top-Down, Constrained-Driven Approach

Iason Vassiliou
Department of EECS
University of California at Berkeley

Qualifying Examination
April 30th, 1997

Current Challenges in Analog System Design

- More analog functions integrated
- Tight performance constraints



Berkeley RF IC group
Integrated receiver

- Increased interaction between blocks - system level trade-offs

➡ Design is harder and more time-consuming

Existing Approaches are Insufficient

- Current approaches
  - ▲"point" tools
  - ▲automatic synthesis
  - ▲integrated environments
  - ▲Top-Down, Constrained-Driven Hierarchical Approach
- Disadvantages
  - ▲component based
  - ▲specialized
  - ▲low complexity
- System-level issues not addressed

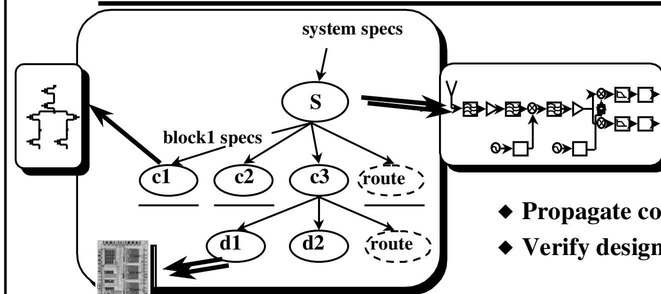
Goals of Proposed Research

- Methodology and tools to accelerate analog system design
- Demonstrate efficiency

Research Proposal

- Explore the realization of the Top-Down, Constraint-Driven Methodology for complex analog systems
  - ▲show the design procedure
  - ▲create new models and tools needed (RF)
  - ▲links to existing tools (optimizers, layout, behavioral simulators)
- Demonstrate the feasibility of efficient system design
  - ▲Video Driver System with programmable PLL
    - −complete implementation and verification
    - −more complex system than other CAD design methodologies
  - ▲RF Systems
    - −develop high-level simulation techniques
    - −start implementation of receiver

Background: Top-Down, Constraint-Driven Hierarchical Design Methodology



(Chang et al 92)

- Propagate constraints
- Verify design bottom-up
- Methodology: procedure + models and tools
  - ▲not fully automatic
- Realized for lower complexity analog components
  - ▲D/A, ΣΔ A/D
- Needs to be expanded for systems

Advantages

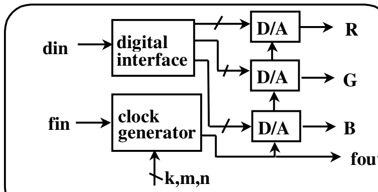
- Design is systematic
- More efficient exploration of design space
- Design errors caught early in design cycle
- Prevent over-design
- Efficient full system verification
- Impact: Faster time-to-market - design less error prone

Methodology for Video Driver System

Goals to achieve

- Design procedure for large commercial system
  - constraint propagation w/optimization
- Use and develop models and layout tools
- Includes PLL - many applications

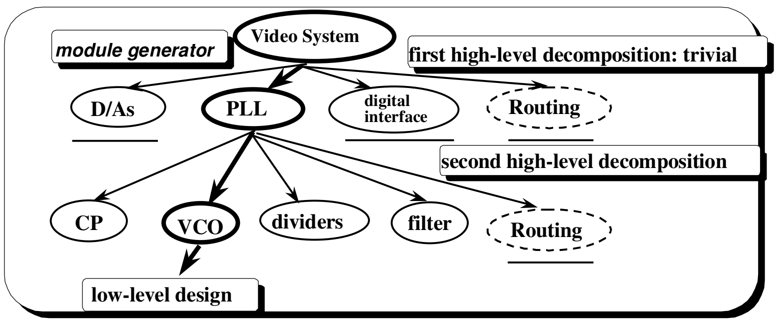
Performance
range: 25MHz - 135MHz
resolution: 8 bits
timing jitter < 1 % rms.
Supply: 5V
Technology: MOSIS HP 1.0u
Power: minimize



"Vehicle" to show methodology for complex mixed-signal systems

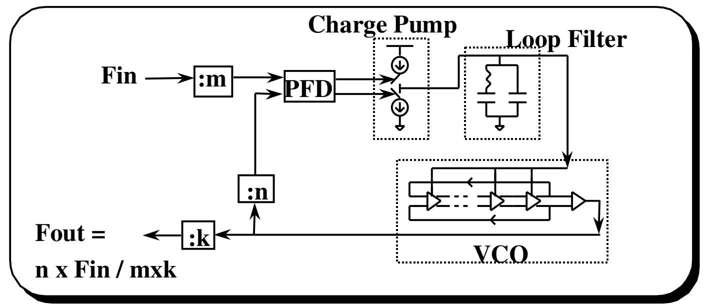
High Level Decomposition

- For the D/As module generators are used
- PLL clock generator: follow methodology to layout



Focus on highlighted "critical" design path

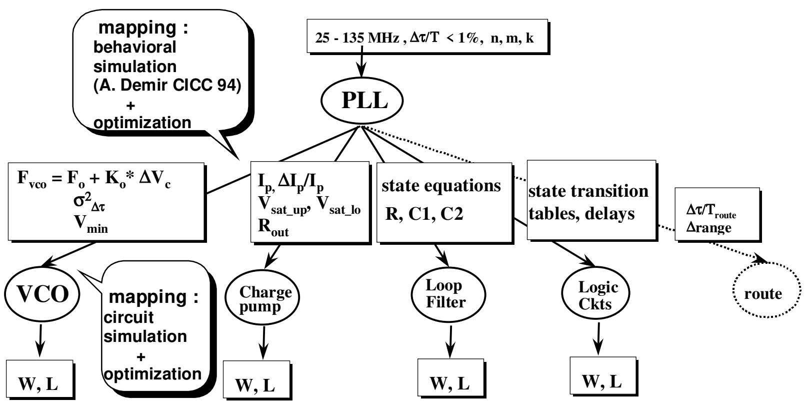
High-Level Design: PLL



- Charge-Pump PLL with ring oscillator VCO
- Fixed F_{ref}, m, n, k to produce given frequencies

Use standard architecture for clock synthesizer

Hierarchical Decomposition/Mapping: PLL

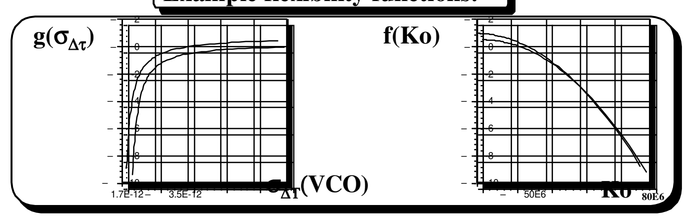


Key contribution:optimization mapping, use of behavioral models

High Level Optimization - 0bjective

- flexibility(Ko , $\sigma^2_{\Delta\tau}$, R , C , Ip) = f(Ko) + g($\sigma^2_{\Delta\tau}$) + h(R) + i(C) + j(Ip) + ...
- Flexibility functions based on
  - ▲design experience
  - ▲circuit equations

Example flexibility functions:



Use flexibility functions as objective

High Level Optimization - Problem Formulation

$$
\begin{array}{ll}
\max & \text{flexibility}(R, C, C_1, I_p, K_O, \ldots) \\
s.t. & T_{acq} \leq T_{max} \\
 & PM_{PLL} \geq 45^{o} \\
 & \Delta T / T_{fmax} \leq 0.7\,\% \\
 & R_L \leq R \leq R_U \\
 & \ldots \\
 & K_{OL} \leq K_O \leq K_{OU}
\end{array}
$$

Constants

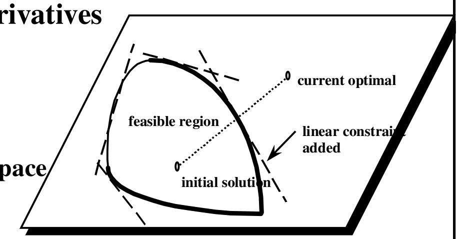
Fo	**100 MHz**
V_{sat_up}	**4.8 V**
V_{sat_lo}	**0.2 V**
$\Delta I_p/I_p$	**5 %**
R_{out}	**2 MΩ**
V_{min}	**1.8 V**
ΔR, ΔC	**20%**
ΔK	**50%**
ΔFo	**30%**

- **Behavioral simulation**
  - ▲**Check worst cases for stability**
  - ▲**Computes jitter if stable**
- **Tolerance to parameter variations**
  - ▲**Phase margin constraint**

Formulate design problem as a non-linear optimization problem

High Level Optimization - Algorithm

- **Most non-linear optimization algorithms require accurate calculation of derivatives**
- **Timing jitter from Monte-Carlo Simulation - inaccurate derivatives**
- **Supporting Hyperplane**
  - ▲**robust enough**
  - ▲**requires 1st derivative only**
  - ▲**derivatives only in feasible space**
  - ▲**works with noisy gradients**
  - ▲**requires convexity**
  - ▲**provide initial point**



High Level Optimization - Results

objective	
flexibility = 2.79	

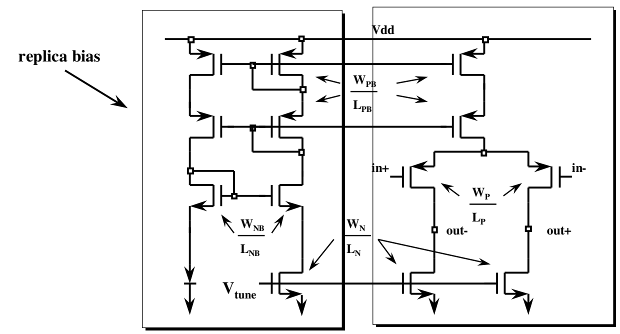
constraint	value
$jitter_{140MHz}$	0.7%
phase margin	44^{O}

Parameter	Value
R	200.5k
C	57.8pF
C1	5pF
Ip	15.8uA
$\Delta\tau_{VCO}$ (140MHz)	3.33ps
Ko	40MHz/V

Iterations	8
CPU	7600 sec (DEC Alpha)

Low-Level Design: VCO

- 8 stage ring oscillator VCO
- Use differential cells to reject supply noise



(similar to D. Reynolds ISSCC 94)

Low Level Optimization - VCO

$$\min \quad Power(Wi, Li, \ldots)$$
$$s.t. \quad \Delta T_{VCO_{140\,MHz}} \leq 3ps$$
$$F_{MAX} - \Delta F_{MAX} \leq F_{MAX} \leq F_{MAX} + \Delta F_{MAX}$$
$$F_{MIN} - \Delta F_{MIN} \leq F_{MIN} \leq F_{MIN} + \Delta F_{MIN}$$
$$V_{MIN} \leq V_1 , \quad V_2 \leq V_{MAX}$$
$$\left[s_c^P\right]^T \bullet \Delta \mathbf{C}_{max} \leq \Delta \mathbf{P}_{max}$$
$$Wi_L \leq Wi \leq Wi_U , \; Li_L \leq Li \leq Li_U$$

Key idea : use sensitivities and parasitics estimate

Constants

L_{nb}, L_{pb}	1 u
W_{pb}	20 u
W_{nb}	10 u
ΔC_{Lmax}	50 %
ΔC_L	15 fF

- ✓ **Fmin, Fmax: simulation (Spice)**
- ✓ **ΔT_{VCO} : equations (Weigandt94)**
- ✓ **Algorithm : Supporting Hyperplane**

Results

◆**Wn**	**2.6u**
◆**Ln**	**4u**
◆**Wp**	**36u**
◆**Lp**	**1u**

2070 CPU sec (DEC Alpha)

Layout

Layout Specifications (sizes, parasitics)

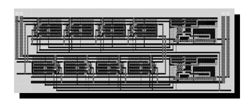
Parasitic Constraint Generation

Constraint Driven Layout Synthesis

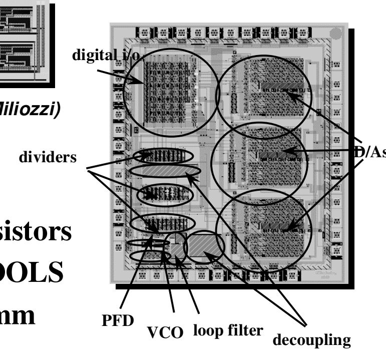
Parasitic Extraction

Constraints Respected?

● **Module Generation: VCO**



(w/ E. Charbon, P. Miliozzi)

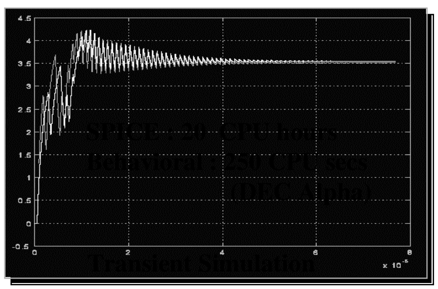


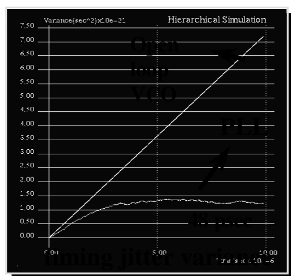
- ◆ **~20,000 transistors**
- ◆ **used OCTTOOLS**
- ◆ **3.4mm x 3.9mm**

use constraint-driven layout - contribute to development of module generator

Bottom-up Verification

- **Bottom-up verification performed**
  - ◆**individual components at circuit level: Spice, noise simulator (Demir ICCAD94)**
  - ◆**PLL using behavioral simulation with extracted parameters**

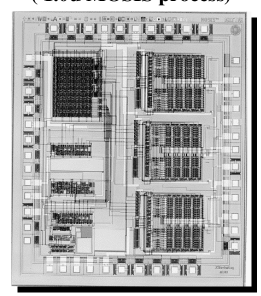




Behavioral simulation: accurate and orders of magnitude faster!

Experimental Results

Chip fabricated
(1.0u MOSIS process)

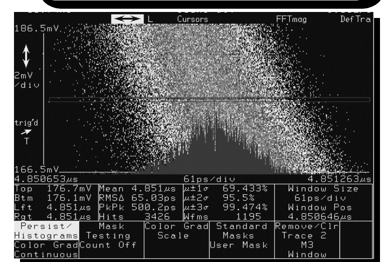


PCB fabricated

Measurements

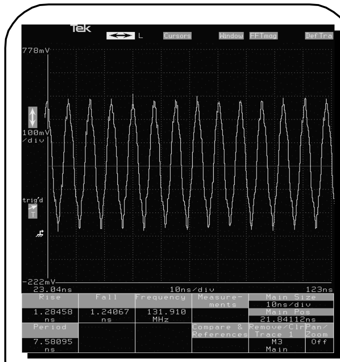
D/A
- ◆**INL 0.15 LSB**
- ◆**DNL 0.05 LSB**
- ◆**Settling time (2%) 6ns**

PLL
- ◆**Range 5Mz - 130 MHz**
- ◆**Jitter 0.65% @100MHz (65 ps)**



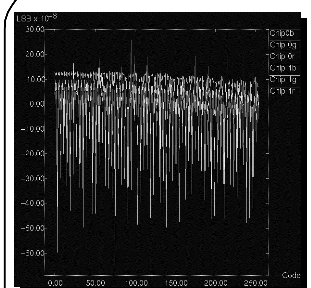
Jitter histogram

Experimental Results (cont)

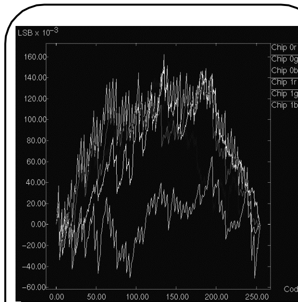


Clock output waveform

Experimental Results (cont)



D/A INL



D/A DNL

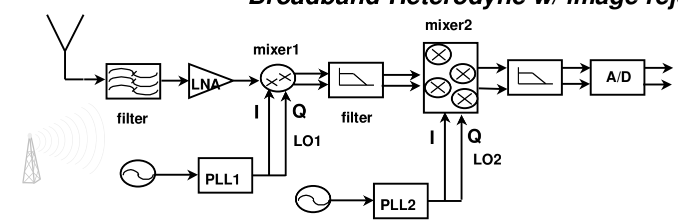
Conclusions from Video Driver Application

- **Developed models and techniques to apply top-down methodology in a complex mixed-signal system**
- **Illustrated design procedure**
  - ▲**specifications to working fabricated parts (first design)**
- **Higher complexity system than other CAD approaches**

Presented at ICCAD '96 (I. Vassiliou, H. Chang et al) -
Chapter on book on top-down design methodology for analog (KAP '97)

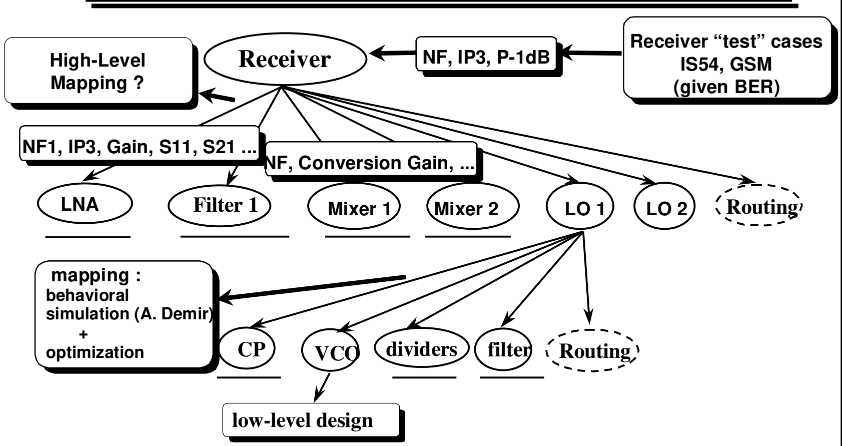
Application 2: RF Systems

Broadband-Heterodyne w/ image rejection



- **State-of-the art analog systems**
- **Key contributions**
  - ▲**new models and high-level simulation techniques**
  - ▲**show design procedure**
    - −**work closely with IC group for CMOS receiver implementation**

RF System: High-Level Decomposition



Typical RF receiver decomposition: Need high level models/simulation techniques

RF Systems: High-Level Design Approaches

- **Use “spreadsheet” with cascade formulas:**

$$NF_{TOTAL} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots + \frac{NF_N - 1}{G_1 G_2 \ldots G_{N-1}}$$

$$\frac{1}{IP_{3_{TOTAL}}} = \frac{1}{IP_{3_1}} + \frac{G_1}{IP_{3_2}} + \frac{G_1 \cdot G_2}{IP_{3_3}} + \ldots + \frac{G_1 \cdot G_2 \ldots G_{N-1}}{IP_{3_N}}$$

- **Rough approximation**
- **Some effects ignored (feedback, phase cancellation, coupling etc.)**
- **Overdesign - Example: IM3 cancellation**
- **Need more efficient technique: from RF models and system specifications get total SNDR**

RF Systems: High-Level Simulation: Desired Properties

- Describe behavior of analog block as a black box
- Independent of implementation details
- Include not only the first-order behavior but also analog second-order effects
  - noise
  - distortion
  - statistical variations

RF High-Level Simulation: Possible Solutions

- Transient simulation using Macro-models
  - do not depend on # of harmonics
  - can be implemented with current simulators
  - depend on implementation
  - complicated modeling of frequency-dependent non-linearities
  - may have convergence problems
- Harmonic Balance
  - need differential equation model
  - exponential complexity w/ # harmonics
- Volterra I/O map for N-ports with harmonic balance

Volterra Series approach (frequency domain)

- **Basic Idea: Volterra series extended to n-ports** **(D. Weiner 76)**
  - ▲**Assuming: N ports, K input harmonics, M-th order non-linearities, $x_1 \ldots x_n$ inputs $y_1 \ldots y_n$ outputs**

$$\overline{\mathbf{x(t)}} = \sum_{q=1}^{K} \overline{\mathbf{x_k}} \cdot e^{j2\pi fkt}, \quad \overline{\mathbf{x_k}} = [x_{1k},\ldots x_{Nk}]^T$$

$$y_n(t) = \sum_{m=1}^{M} y_n^{(m)}(t),$$

$$y_n^{(m)}(t) = \sum_{\substack{n_1,\ldots n_m \\ k_1,\ldots,k_m}} H^{(m)}_{nn_1\ldots n_m}(f_{k1},\ldots,f_{km}) \cdot x_{n1}(f_{k1})\cdot\ldots\cdot x_{nm}(f_{km}) \cdot e^{j2\pi(fk1+\ldots+fkm)t}$$

Strong Non-linearities

- **Assuming periodically-driven strong non-linearities "sideband" transfer functions can be used**
  - ▲**Periodically-driven with frequency LO, harmonic input:**

LTV system:

$$y(t) = \int_{-\infty}^{\infty} h_1(t;\tau_1)\cdot x(\tau_1)\, d\tau_1$$

assuming h(t) periodical (mixers - periodical excitation)
fourier transform- harmonic input $x_f e^{j2\pi f}$

frequency domain:

$$y(t) = \sum_{l=-\infty}^{\infty} H^{l}(f)\cdot x_f e^{j2\pi(f+l\cdot f_{LO})t}$$

⇒can also be applied to strong non-linearities due to large input assuming periodic signals

Strong Non-linearities (cont.)

- Expand to Volterra: weakly non-linear, periodically time-varying system (mixer w/ disto)

$$y(t) = \int_{-\infty}^{\infty} h_1(t;\tau_1)\cdot x(\tau_1)\,d\tau_1 + \ldots + \int_{-\infty}^{\infty}\ldots\int_{-\infty}^{\infty} h_n(t;\tau_1,\ldots,\tau_n)\cdot x(\tau_1)\ldots x(\tau_n)\,d\tau_1\ldots d\tau_n$$

(Flake 63, Rice 73, Swerdlow 78)

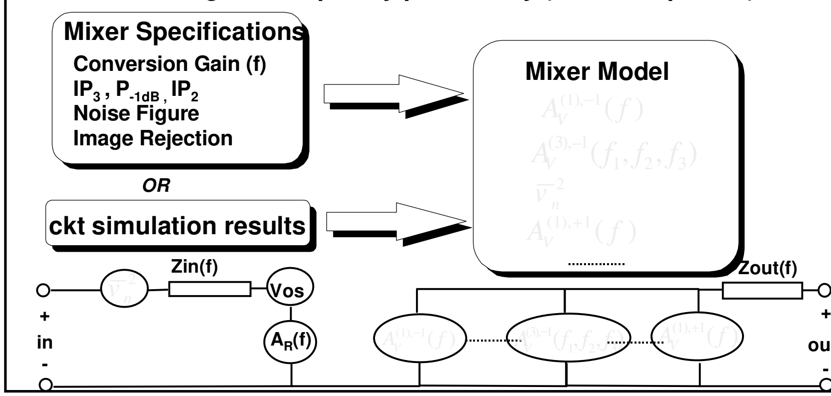
Harmonic inputs - multiple fourier transform

Few non-zero

$$y_n^{(m)}(t) \;=\; \sum_{n1=1}^{N}\ldots\sum_{nm=1}^{N}\;\sum_{k1=1}^{K}\ldots\sum_{km=1}^{K}\;\sum_{l=-L}^{L} \boxed{H^{(m),l}_{n n_1\ldots n_m}(f_{k1},\ldots,f_{km})}\cdot x_{n1}(f_{k1})\ldots x_{nm}(f_{km})\cdot e^{j2\pi(fk1+\ldots+fkm+l\cdot f_{LO})t}$$

Key Contribution: New RF High-Level Models

✓Sum of complex sources, impedences, volterra kernels
✓Defined at given frequency points only (I/O look-up table)



New High-Level Simulation Approach

- **Determine output harmonics:**

$$f_j = \sum_{i=1}^{K} m_i \cdot f_i + \sum_{i=1}^{L} l_i \cdot f_{LOi}, \quad \forall m_i,\, l_i: \quad \sum_{i=1}^{K} |m_i| \le M_{\max}, \quad \sum_{i=1}^{L} |l_i| \le L_{\max},$$

  - ▲f_i: weak inputs, f_{LOi}: strong nonlinearities

- **Formulate network equations:**
  - ▲(2b+n) x J equations and unknowns

$\forall f_j$:

KCL: $\mathbf{A} \cdot \overline{\mathbf{i}(f_j)} = \mathbf{0}$

KVL: $\overline{\mathbf{v}(f_j)} - \mathbf{A}^T \cdot \overline{\mathbf{e}(f_j)} = \mathbf{0}$

$$\sum_{i,l:f_i+q_l f_{LO_l}=f_j} \mathbf{K}_I^{(1)q_l f_{LO_l}}(f_i) \cdot \mathbf{i}(f_i) + \sum_{i,l:f_i+q_l f_{LO_l}=f_j} \mathbf{K}_V^{(1)q_l f_{LO_l}}(f_i) \cdot \mathbf{v}(f_i) + \ldots$$
$$\sum_{\substack{i1,i2,i3,l:\\ f_{i1}+f_{i2}+f_{i3}+q_l f_{LO_l}=f_j}} \mathbf{K}_V^{(3)q_l f_{LO_l}}(f_{i1}, f_{i2}, f_{i3}) \cdot \mathbf{v}(f_{i1}) \otimes \mathbf{v}(f_{i2}) \otimes \mathbf{v}(f_{i3}) = \mathbf{S}(f_j)$$

Generalized branch equations for every harmonic

High-Level Simulation Approach (cont.)

- **Formulate "harmonic balance" nonlinear system of equations:**

$$\mathbf{Q}^{(1)} \cdot \mathbf{x} + \mathbf{Q}^{(2)} \cdot \mathbf{x} \otimes \mathbf{x} + \mathbf{Q}^{(3)} \cdot \mathbf{x} \otimes \mathbf{x} \otimes \mathbf{x} = \mathbf{S}$$

$$\text{where } \mathbf{x} = \begin{bmatrix} \mathbf{i}(f_1) \\ \ldots. \\ \mathbf{i}(f_J) \\ \mathbf{v}(f_1) \\ \ldots \\ \mathbf{v}(f_1) \\ \mathbf{e}(f_1) \\ \ldots \\ \mathbf{e}(f_1) \end{bmatrix} \text{ and } \mathbf{Q}^{(i)} \text{ are assembled from } K_{V,I}^{(m),l}$$

Very Sparse !

•similar approach: VIOMAP(Verbeyst 94)
- *•only for weakly nonlinear*
- *•cascade*

- **Solve non-linear system using Newton-Raphson**
- **Problem: exponential complexity**
  - ▲ok for small RF behavioral systems
- **Noise simulation : use only 1st order sidebands**

Status

- Finished implementation of video driver example
- ➡ RF simulator implementation
- Test simulator to real designs
- Start implementation of GSM receiver
  - ▲high-level design
  - ▲use/develop existing modules
  - ▲work w/ IC group for full implementation

Summary of Contributions

- Developed techniques to apply top-down, constraint-driven design methodology in complex systems
  - ▲behavioral models and optimization-based mapping(PLL)
  - ▲behavioral simulation and modeling (RF)
  - ▲shown design procedure for complex systems
- Demonstrated feasibility of efficient system design
  - ▲Video Driver System - complete implementation
    - Fabricated parts worked the first time
  - ▲GSM receiver
    - Explore high-level design trade-offs, start implementation
- Impact: Easier, more systematic analog system design