Amit Mehrotra

Citizenship: Indian
Visa: F1

Address:
University of Illinois at Urbana Champaign
412 Computer & Systems Research Laboratory
1308 West Main St
Urbana, IL 61801 USA

Office: 217 265 8236
Fax: 217 244 1946
Email: amehrotra@uivlsi.csl.uiuc.edu
URL: http://www.ece.uiuc.edu/fachtml/mehrotra.html

Research Interests

Radio Frequency (RF), analog and mixed signal circuit design, simulation techniques for RF and mixed signal circuits and systems, interconnect performance and modelling issues in VLSI and novel circuits and physical design issues for high performance DSM VLSI designs.

Academic Employment

August 1999	Assistant Professor of Electrical and Computer Engineering	University of Illinois at Urbana-Champaign

Education

Ph.D. University of California, Berkeley, USA – December 1999

Major: Electrical Engineering and Computer Sciences
Thesis: Simulation and Modelling Techniques for Noise in Radio Frequency Integrated Circuits
Advisor: Professor Alberto L Sangiovanni-Vincentelli

M.S. University of California, Berkeley, USA – December 1996

Major: Electrical Engineering and Computer Sciences
Thesis: Hybrid Josephson-CMOS FIFO
Advisor: Professor Theodore Van Duzer

B. Tech. Indian Institute of Technology, Kanpur, India – May 1994

Major: Electrical Engineering
Project: Design of Clock Extraction Circuit for 300 Mbps Communication Receiver
Advisors: Professor Aloke K Dutta and Professor Joseph John

Research Experience

Graduate Student Researcher, Electronics Research Laboratory, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley.

December 1996 – July 1999: Research in

- Noise analysis in radio frequency integrated circuits
- Logic minimization for sequential circuits
- Physical design for deep sub-micron integrated circuits

January 1995 – December 1996:

- Research in CMOS circuits for cryogenic temperature operation

Teaching Experience

Spring 2000: Course Director and Instructor for ECE383 *Integrated Circuit Design.*

Fall 1999: Course Instructor for ECE342 *Electronic Circuits.*

Fall 1997: Graduate Student Instructor for EECS 219A *Computer Analysis of Electrical Circuits.* Instructor: Professor Alberto L Sangiovanni-Vincentelli. Taught classes, set and graded homeworks, examinations and projects.

Fall 1994: Graduate Student Instructor for EECS 43 *Introductory Electronics Laboratory.* Instructor: Professor William Oldham. Conducted lab and office hours.

Industry Experience

Internships at

- Bell Laboratories, Lucent Technologies, Murray Hill, NJ, USA. Summer 1997
- Rockwell Semiconductor Systems, Newport Beach, CA, USA. Summer 1996
- Sun Microsystems, Sunnyvale, CA, USA. Summer 1995

Administrative Experience

- Served on the Undergraduate Curriculum Committee at University of Illinois at Urbana-Champaign (Fall 1999).
- Wrote regular progress reports and grant proposals to the Semiconductor Research Consortium. Interacted with SRC members from IBM, Texas Instruments, Bell Laboratories, Motorola, etc.
- Presented research at Annual SRC review meetings at Texas Agricultural and Mechanical University, College Station, TX, USA (1997), Carnegie Mellon University, Pittsburgh, PA, USA (1998) and Georgia Institute of Technology, Atlanta, GA, USA (1999).

Honours and Awards

- Outstanding Paper Award, International Conference of Computer Design (ICCD) 1997,
  - Architecture and Algorithms Track for "Benchmarking and Analysis of Architecture for CAD Applications"
- The President's Gold Medal (Graduating Class 1994), Indian Institute of Technology, Kanpur, India
- Academic Excellence Award, Indian Institute of Technology, Kanpur, India 1990–1994
- National Talent Search Scholarship, National Council of Educational Research and Training, India, 1988-94

Reviewing

- International Symposium on Circuits and Systems 2000
- Custom Integrated Circuits Conference 1999
- Design Automation Conference 1998 & 1999
- International Conference on Computer Aided Design 1997, 1998 & 1999
- International Conference on Computer Design 1997 & 1998

Publications

Published Papers

1. "Quantitative Projections of Reliability and Performance for Low-k/Cu Interconnect Systems", Kaustav Banerjee, Amit Mehrotra, William Hunter, Krishna C Saraswat and S Simon Wong, *to appear in Proceedings, International Reliability Physics Symposium*, 2000.

2. "Phase Noise in Oscillators: A Unifying Theory and Numerical Methods for Characterization," Alper Demir, Amit Mehrotra and Jaijeet Roychowdhury, *to appear in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications.*

3. "Noise Analysis of Non-Autonomous Radio Frequency Circuits", Amit Mehrotra and Alberto Sangiovanni-Vincentelli, *to appear in IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, 1999.

4. "A Noise-Immune VLSI Layout Methodology with Highly Predictable Parasitics," Sunil Khatri, Amit Mehrotra, Robert Brayton, Ralph Otten and Alberto Sangiovanni-Vincentelli, *Proceedings, 36th Design Automation Conference*, pp. 491–496, 1999.

5. "On Thermal Effects in Deep Sub-Micron VLSI Interconnects", Kaustav Banerjee, Amit Mehrotra, Alberto Sangiovanni-Vincentelli and Chenming Hu, *Proceedings, 36th Design Automation Conference*, pp. 885–891 1999.

6. "Phase Noise in Oscillators: A Unifying Theory and Numerical Methods for Characterization," Alper Demir, Amit Mehrotra and Jaijeet Roychowdhury, Proceedings, *Proceedings, 35th Design Automation Conference*, pp. 26–31, 1998.

7. "Phase Noise and Timing Jitter in Oscillators," Alper Demir, Amit Mehrotra and Jaijeet Roychowdhury, *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 45–48, 1998.

8. "Phase Noise in Oscillators," Alper Demir, Amit Mehrotra and Jaijeet Roychowdhury, *Proceedings, International Symposium on Nonlinear Theory and Its Applications*, pp. 517–520, 1997.

9. "Sequential Optimization without State Space Exploration", Amit Mehrotra, Shaz Qadeer, Vigyan Singhal, Robert Brayton, Alberto Sangiovanni-Vincentelli and Adnan Aziz, *International Conference on Computer Aided Design, Digest of Technical Papers*, pp. 208–215, 1997.

10. "Benchmarking and Analysis of Architectures for CAD Applications", Amit Mehrotra, Shaz Qadeer, Rajeev Ranjan and Randy Katz, *Proceedings of the International Conference on Computer Design*, pp. 670–675, 1997.

11. "Sequential Optimization without State Space Exploration", Robert Brayton, Amit Mehrotra, Shaz Qadeer and Vigyan Singhal, *Proceedings International Workshop on Logic Synthesis*, 1997.

12. "Benchmarking and Analysis of Architectures for CAD Applications", Amit Mehrotra, Shaz Qadeer, Rajeev Ranjan and Randy Katz, *Proceedings International Workshop on Logic Synthesis*, 1997.

13. "Status of research on Josephson-CMOS circuits for 4 K operation," Theodore Van Duzer, Seendripu Kishore, Luong Huynh, David Hebert, Amit Mehrotra, Uttam Ghoshal and Steven Whiteley, *Proceedings EUCAS, the Second European Conference on Applied Superconductivity*, 1995.

Technical Reports

14. "Routing Techniques for Deep Sub-Micron Technologies", Sunil Khatri, Amit Mehrotra, Mukul Prasad, Robert Brayton and Alberto Sangiovanni-Vincentelli, UC Berkeley Electronics Research Laboratory, Memorandum No. UCB/ERL M99/15, 1999.

15. "Simulation Techniques for Noise in Non-Autonomous Radio Frequency Circuits," Amit Mehrotra and Alberto Sangiovanni-Vincentelli, UC Berkeley Electronics Research Laboratory, Memorandum No. UCB/ERL M99/10, 1999.

16. "A Noise-Immune VLSI Layout Methodology with Highly Predictable Parasitics," Sunil Khatri, Amit Mehrotra, Robert Brayton, Ralph Otten and Alberto Sangiovanni-Vincentelli, UC Berkeley Electronics Research Laboratory, Memorandum No. UCB/ERL M98/24, 1998.

Papers in Submission

17. "Sequential Optimization without State Space Exploration", Amit Mehrotra, Shaz Qadeer, Vigyan Singhal, Robert Brayton, Alberto Sangiovanni-Vincentelli and Adnan Aziz, *submitted to IEEE Transactions on Computer-Aided Design.*

18. "Impact of Thermal Effects on the Reliability and Performance of Deep Sub-Micron VLSI Interconnects", Kaustav Banerjee and Amit Mehrotra, *submitted to IEEE Journal of Solid State Circuits.*

19. "Performance Analysis of Interconnect Architectures for 3D ICs", Shukri J Souri, Kaustav Banerjee, Amit Mehrotra, Krishna C Saraswat and S Simon Wong, *submitted to Design Automation Conference*, 2000.

Invited Lectures/Seminars

1. "Phase Noise Analysis of Electrical Oscillators", Rockwell Semiconductor Systems, December 1997.

2. "Simulation and Modelling Techniques for Noise in Radio Frequency Integrated Circuits", Electrical and Computer Engineering Department, University of Texas at Austin, March 1999.

3. "Simulation and Modelling Techniques for Noise in Radio Frequency Integrated Circuits", Electrical and Computer Engineering Department, University of Illinois at Urbana-Champagne, May 1999.

4. "Simulation and Modelling Techniques for Noise in Radio Frequency Integrated Circuits", IBM TJ Watson Research Center, Yorktown Heights, May 1999.