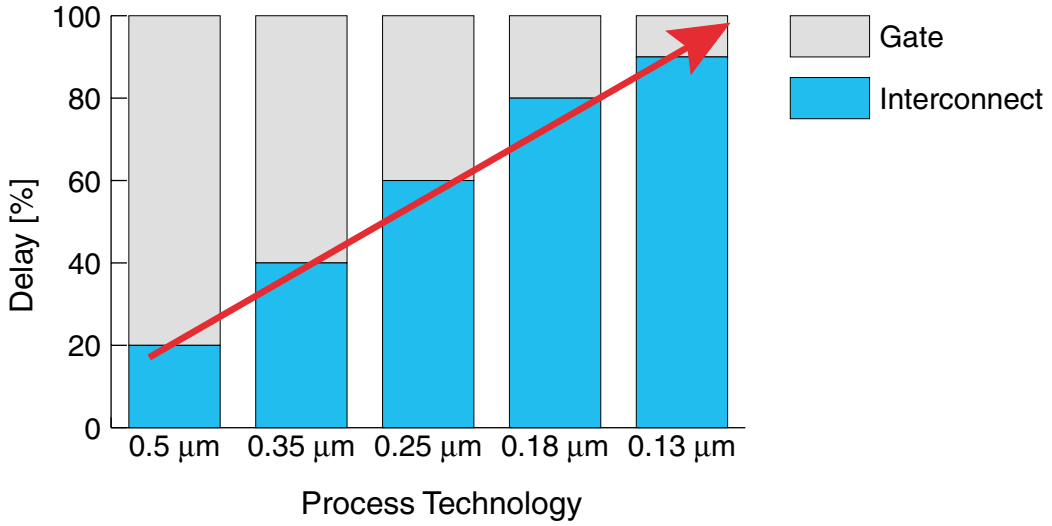
presents

High-Speed High-Accuracy 3D VLSI Extraction

Motivation

- **Interconnects Now Dominate VLSI**
  - Timing
  - Signal Integrity



- **Existing Interconnect Extractors Fail**
  - Poor Accuracy & High Speed
  - Medium Accuracy & Very Low Speed
- **Need High-Speed High-Accuracy Extractor**

Overview

- Company
- Technology
  - High-speed High-accuracy BEM 3D Field Solver
  - Efficient Net-by-Net RC Extraction
- Products
  - Extraction of Critical Cells, Blocks, Nets
  - Distributed RC Models
  - IR drop
  - Substrate Coupling
- Differentiation
  - 2D / 2.5D / 3D Tools
- Summary

Coyote Systems

- **History**
  - **Privately held, located in San Francisco CA**
  - **Founded in July 1996 by 3D Field Solver & MEMS experts**
  - **DARPA contract to develop extremely fast & easy-to-use 3D CAD for MEMS**
- **Products**
  - **First MEMS product AutoMEMS® announced July 1998**
  - **First VLSI product AutoIC® announced June 1999**
  - **New Tools**
    - AutoIC® v2, AutoIC-SMP™, AutoNet™, AutoSubstrate™, AutoIRdrop™, AutoMEMS® v2
- **Customers**
  - **End-users include Siemens, Monterey, Analog Devices, Motorola, Texas Instruments, Hewlett-Packard, Sandia, MIT, Berkeley, CMU**
  - **OEM licenses include Monterey Design**

Company Mission

- **VLSI**

  Provide premium high-speed high-accuracy solutions for extraction, timing, and signal integrity problems for modern VLSI designs.

- **MEMS**

  Provide premium high-speed high-accuracy analysis of large, realistic MEMS devices.

Coyote Products

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Technology

AutoBEM	Fastest BEM field solver
AutoBEM-SMP	Exploit fine-grained parallelism on SMP computers

VLSI

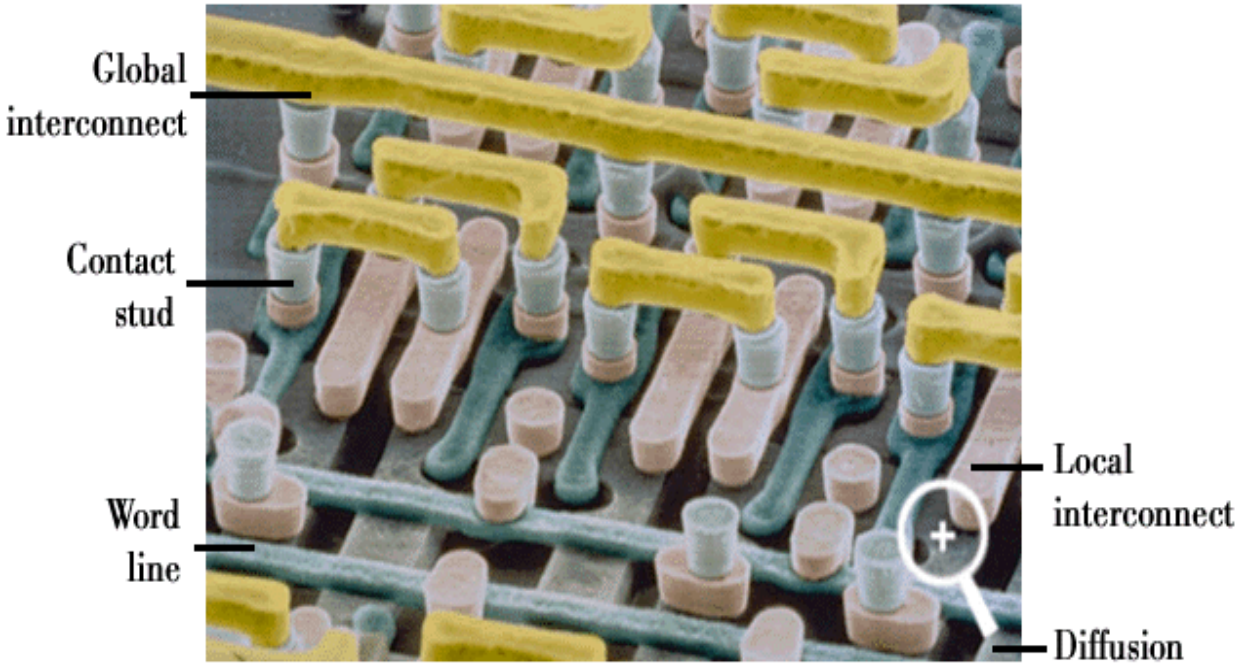
AutoIC	Capacitance extraction of interconnects
AutoIC-SMP	SMP support
AutoNet	Distributed RC models from layout
AutoSubstrate	Resistive coupling in substrate
AutoIRdrop	Potential drop in powergrid

MEMS

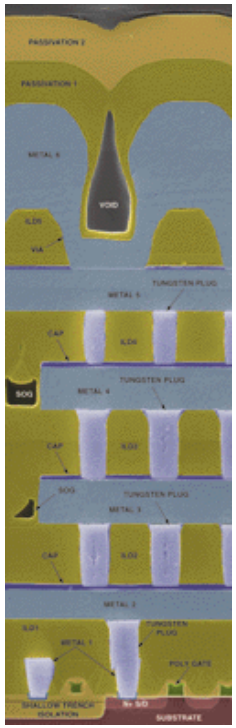
AutoMEMS	Coupled electro/mechanical simulator
AutoMEMS-SMP	SMP support

VLSI Geometries

- Interconnects dominate performance
- Deep submicron is 3D
  - Huge layouts
  - Intricate topologies



- IBM



- AMD

VLSI Extraction

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- **RC Interconnect Extraction Tools**
  - **High-Speed**
  - **High-Throughput**
  - **High-Capacity**
  - **High-Accuracy**

- **Possible Alternatives**
  - **3D Field Solvers**
    - Coyote Systems
    - Raphael™
    - FastCap
  - **Statistical Methods**
    - QuickCap™
  - **Pattern Matchers**
    - Simplex
    - Frequency
    - Mentor
    - Ultima

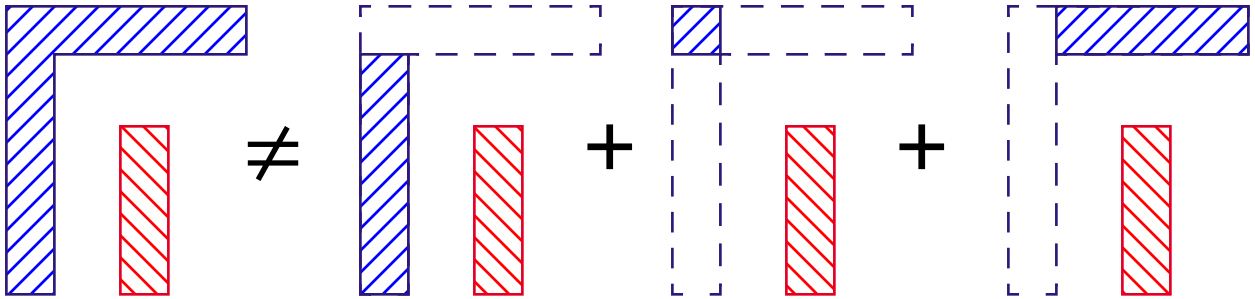
- **Identify Advantages/Disadvantages**

Pattern Matchers

- **Why they are used**
  - **Mature technology, Very Fast**
  - **Requires 3D field solver to develop pattern library**
- **2D/2.5D tools do not capture 3D DSM effects**
  - **Fast (<100,000 nets/hour) after lengthy precharacterization (100-200 hours)**
  - **Increasing difficulties with modern processes**
    - Many Layers, small feature sizes
    - Arbitrary angles & non-manhattan geometries
    - PCB-style variable wire width
    - Increasing number of patterns needed
  - **Optimistic "error cancellation" - no bounded errors**
  - **Large errors (>20%)**

Accuracy Problem!

- Some pattern matching vendors claim <<10% errors
- Simple counterexample...



- 3D simulation reveals 20% errors using superpositioning!
- Geometric non-linearities prevent accurate solutions

Statistical Methods

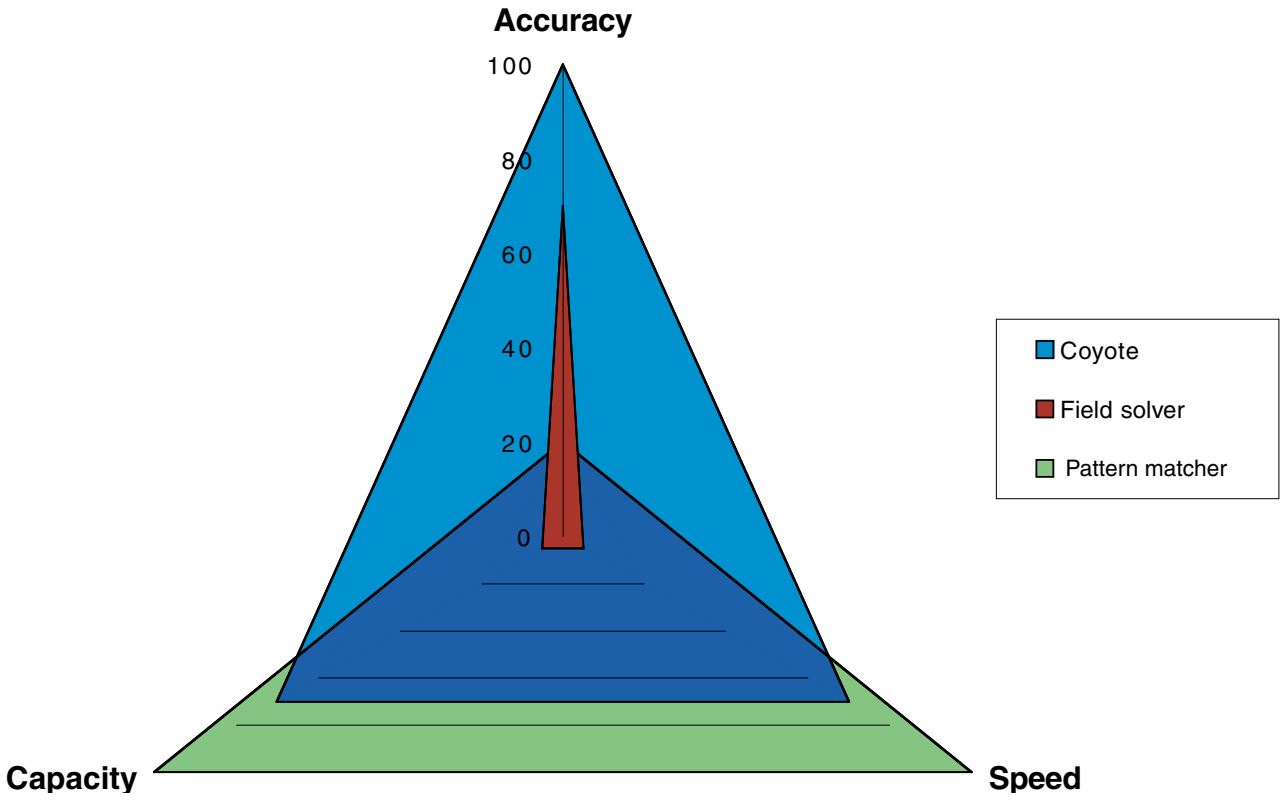
- **Why are they sometimes used**
  - Alternative to FEM, FDM
  - Reasonably good for Self-Cap & Small Problems
- **Why will they not solve the problem**
  - No Distributed R's & C's
  - Very long run times with increasing number of nets
  - Inaccurate Coupling Capacitance - Cij
  - Only supports Manhattan Geometries
  - Expensive support for multiple dielectrics
  - Solves only part of the problem - Cii

Alternative Solvers

- **Proposed Technologies**
  - FEM
  - FDM
  - Traditional BEM
- **Why will they not solve the problem**
  - Not fast enough
  - Limited to very small problems
  - Huge memory and CPU time requirements
- **Computationally not feasible**

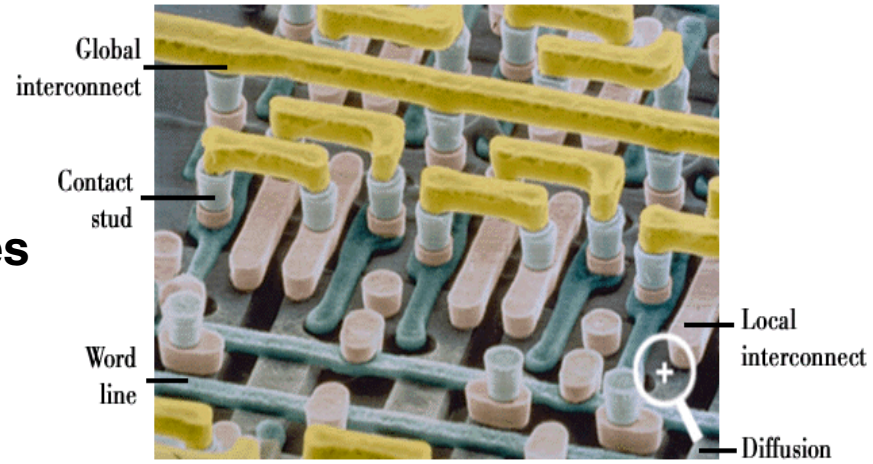
VLSI Extraction

- **Coyote combines advantages of all approaches!**
  - **Field solver accuracy**
  - **Pattern matcher speed & capacity**

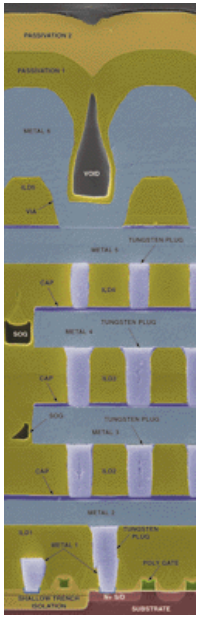


VLSI Geometries

- Interconnects dominate performance
- Deep submicron is 3D
  - High aspect ratios
  - Extreme Density
  - Round Corners
  - Cylindrical Vias
  - Variable width wires
  - Nonideal Cross-Sections
  - IBM



  - AMD



  - Coyote can verify the effect of all these features!
    - Simplex, Frequency, Avanti, Mentor, QuickCap™ cannot
- 3D problems require 3D solutions!

3D Field Solvers

- **Arbitrary Geometries**
  - PCB-style, manhattan & non-manhattan
- **Arbitrary Materials**
  - Planar & conformal dielectrics
- **Arbitrary Boundary Conditions**
  - Neumann, Dirichlet, mixed, floating

- **Only Coyote's AutoIC® solves everything!**
  - AutoIC is faster, more accurate, and easier to use!

3D Field Solvers

- If field solver, then pick best field solver
  - Simplest, smallest model
  - Most accurate (states & gradients)
  - Fastest runtime
  - Lowest memory requirements

	BEM			*FEM*	
	Direct	*Iterative*	*Multipole*	*Direct*	*Iterative*
Nr. nodes	N^2	N^2	N^2	N^3	N^3
Memory	N^4	N^4	(NlogN)^2	N^6	N^4.5
CPUtime	N^6	N^4	(NlogN)^2	N^9	N^4.5

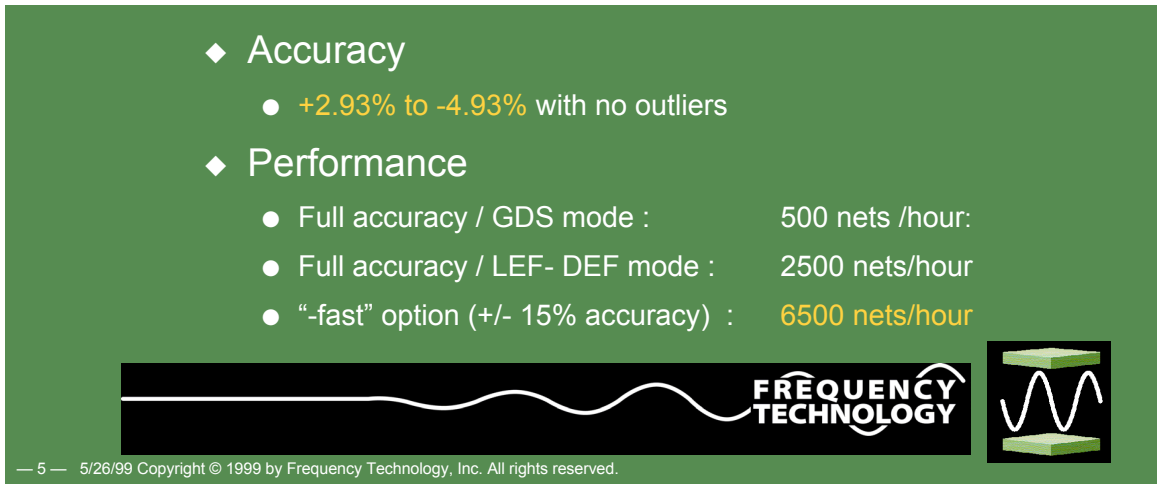
  - Coyote uses Multipole Accelerated BEM
  - Computational Scaling N^2 → NlogN

AutoIC Field Solver

- **VLSI Interconnect Extraction**
  - Accelerated Boundary Element Method
  - Automatic meshed 3D model from 2D layout
  - Adaptive mesh refinement
  - Robust automation
  - Scriptable batch-mode or interactive GUI-mode operation
  - Superset of Sematech extraction API
  - Cluster & symmetric multiprocessing (SMP) support

AutoIC Speed

- **AutoIC™ 3D Field Solver**
  - **2,000,000 BEM elements/hour per cpu**
  - **1,500 nets/hour per cpu** (user selected <2% error)
- **AutoIC vs. Field Solvers**
  - **10-50x faster than QuickCap™**
  - **100-500x faster than Raphael™**
- **AutoIC vs. Library-based "Pattern Matchers"**
  - **Similar speed to Frequency**



AutoIC

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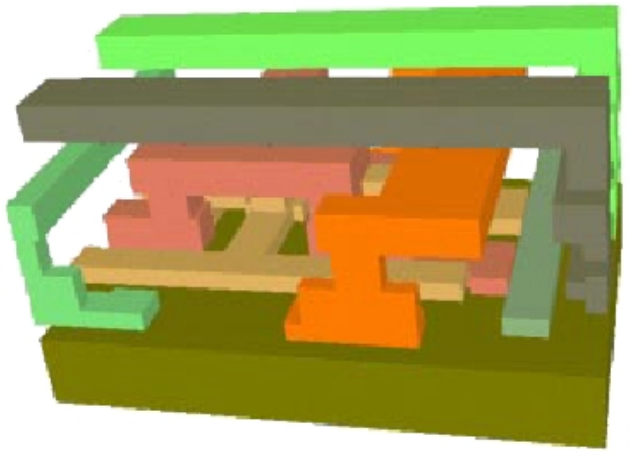
- **Best Performance**
  - Faster than FastCap, QuickCap™, Raphael™, Space, etc.
  - As fast as pattern matchers!
  - Solves many more problems
  - Large savings replacing multiple licenses
  - Large engineering time savings

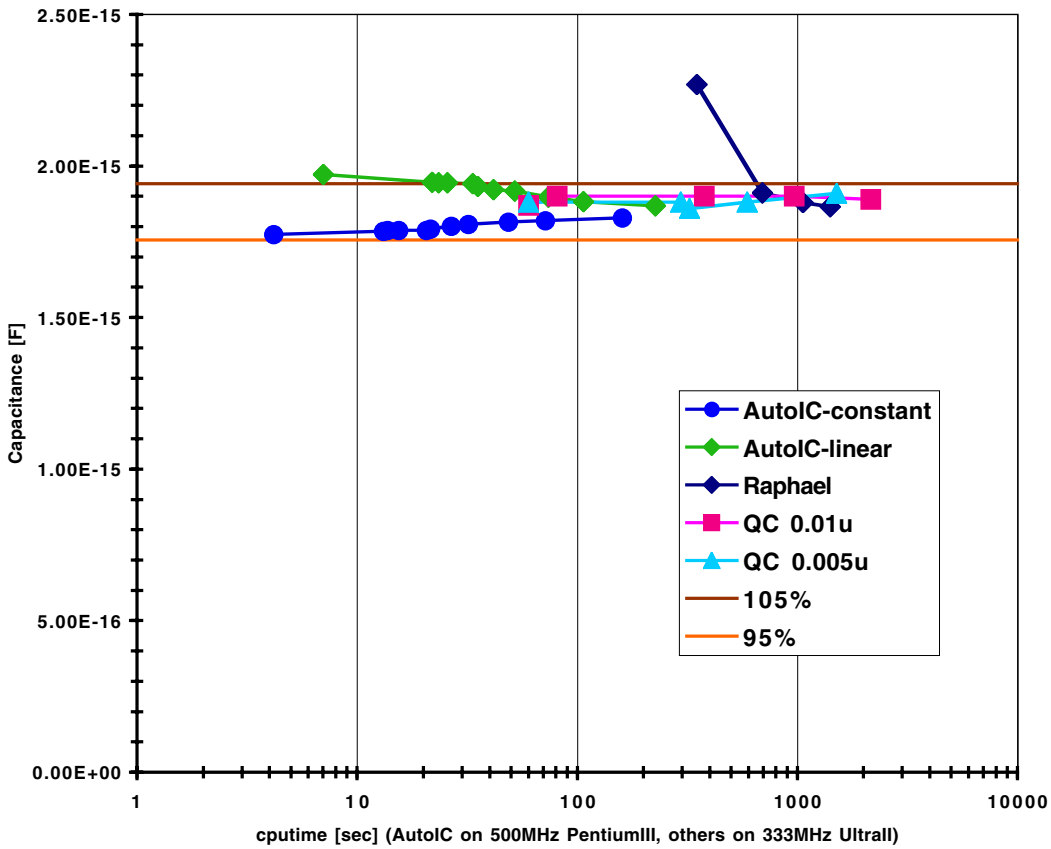
Customer Tests

- **Motorola SRAM Evaluation**
  - Self-cap Extraction
  - Cross-cap Extraction
  - Convergence
  - Time & Memory
  - Model Generation
  - Ease-of-Use
- **Motorola Compared**
  - AutoIC™
  - QuickCap™
  - Raphael™



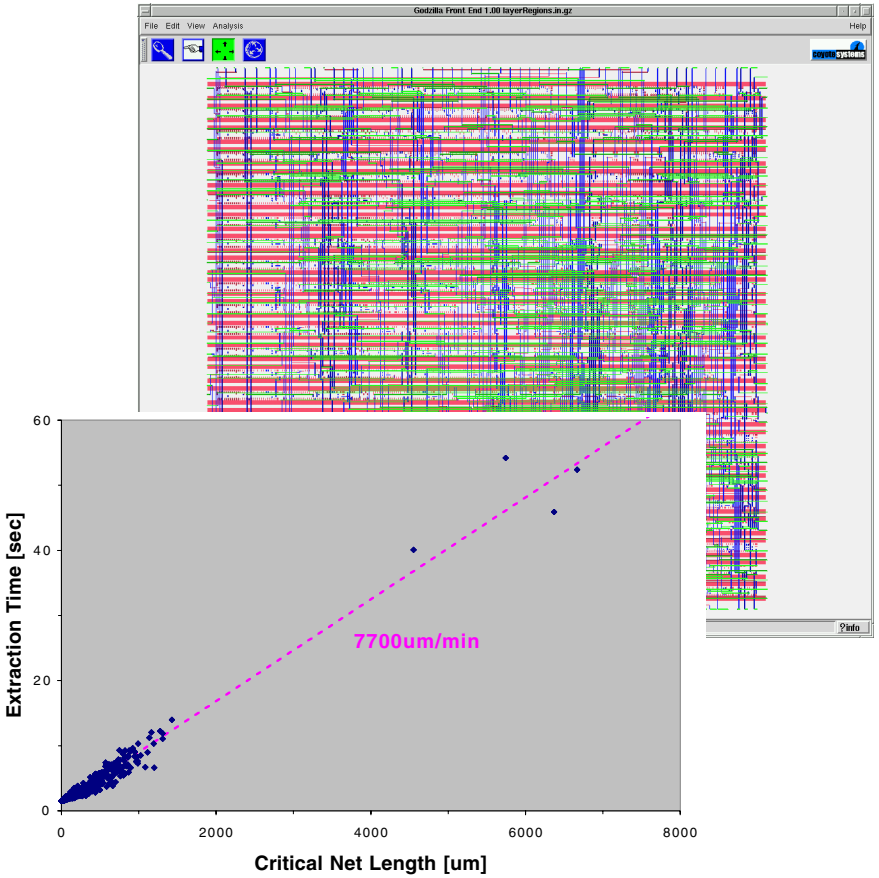
Motorola SRAM Cell

- **Convergence of bit-line self-capacitance**
  - Require better than ±5% accuracy
- **AutoIC**
  - 10-100x faster!
  - Best convergence!
  - Tight error bounds!



Siemens Block

- **Extract Critical Nets**
  - 500 nets
  - 1x1mm die
  - 0.35um process
  - 3 metal layers
  - Multiple dielectrics



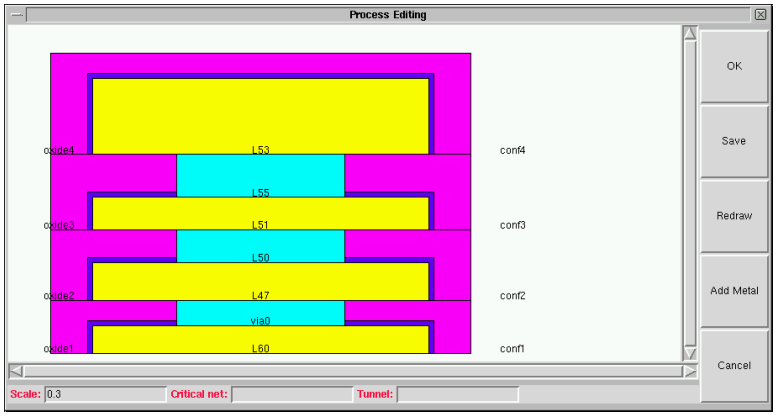
- **AutoIC results**
  - <2% Errors
  - Excellent scaling
  - 8mm/min extraction
  - All nets extracted in 20 min using 1 cpu = 1,500 nets/hour
  - All nets extracted in 1 min using 20 cpus = 30k nets/hour

Design Flow

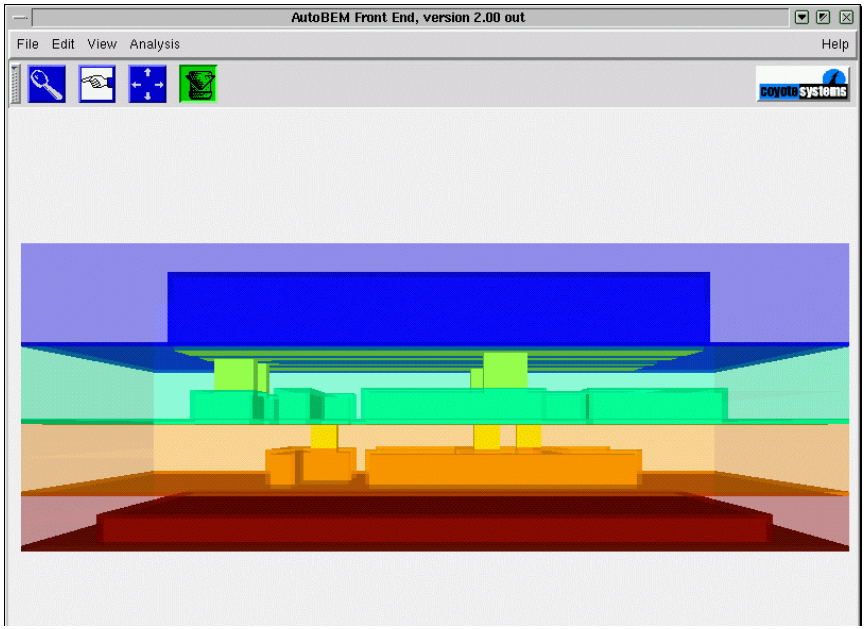
- Industry Std Layout
  - GDSII, annotated GDSII, CIF, Sematech API
- 3D Model Generator
  - Flexible process descriptor
  - API-mode or Batch-mode or GUI-mode
- 3D RC Extraction
  - Lumped, distributed
  - API-mode or Batch-mode or GUI-mode
- Industry Std Output
  - Spice, Sematech API
  - 3D visualization

Model Generation

- **Input**
  - **Layout**
  - **Process Description**
    - Arbitrary layers
    - Interlayer dielectrics
    - Conformal dielectrics

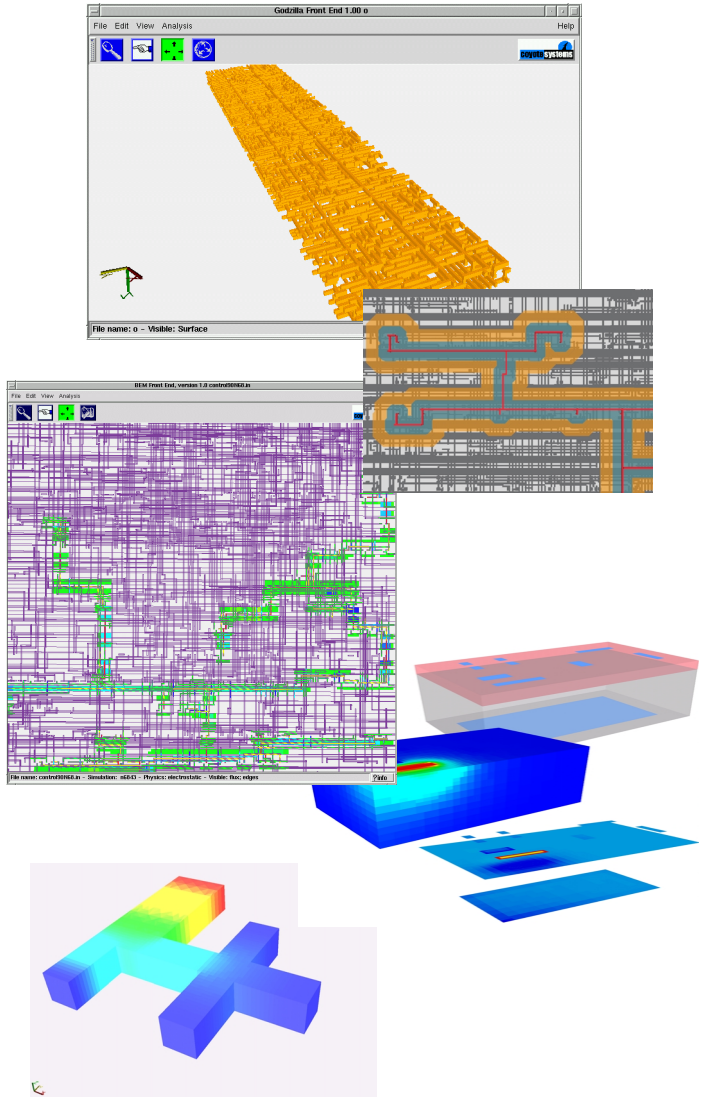


- **Output**
  - **Meshed 3D Model**



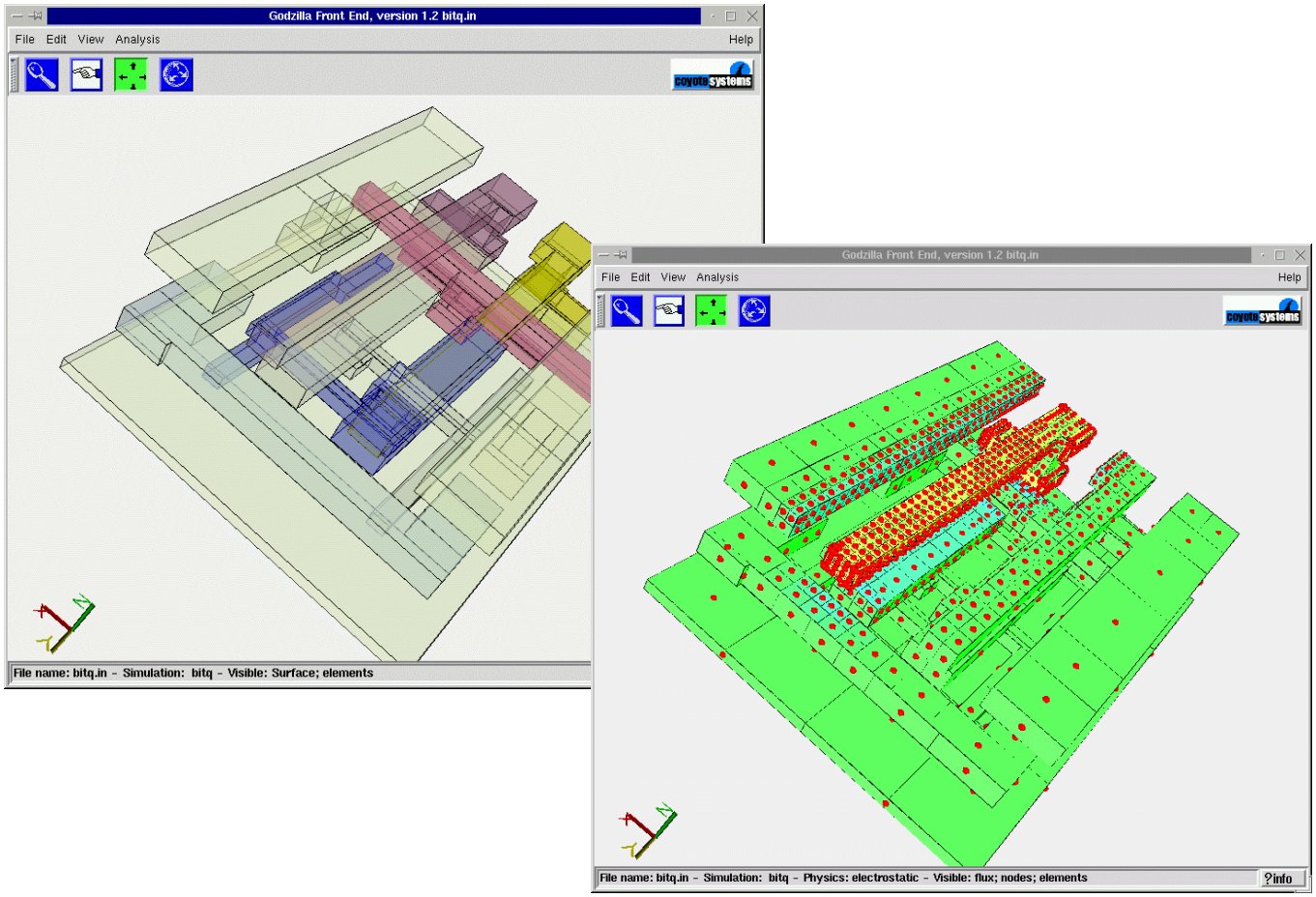
Applications

- **Critical Cells**
  - Coefficient generation
  - Cell optimization
- **Critical Blocks**
  - IP characterization
  - Routing
- **Critical Nets**
  - Clock trees, control lines
  - User-selected nets
- **Substrate Coupling**
- **IR drop**
  - Power grid effects delays



Critical Cells

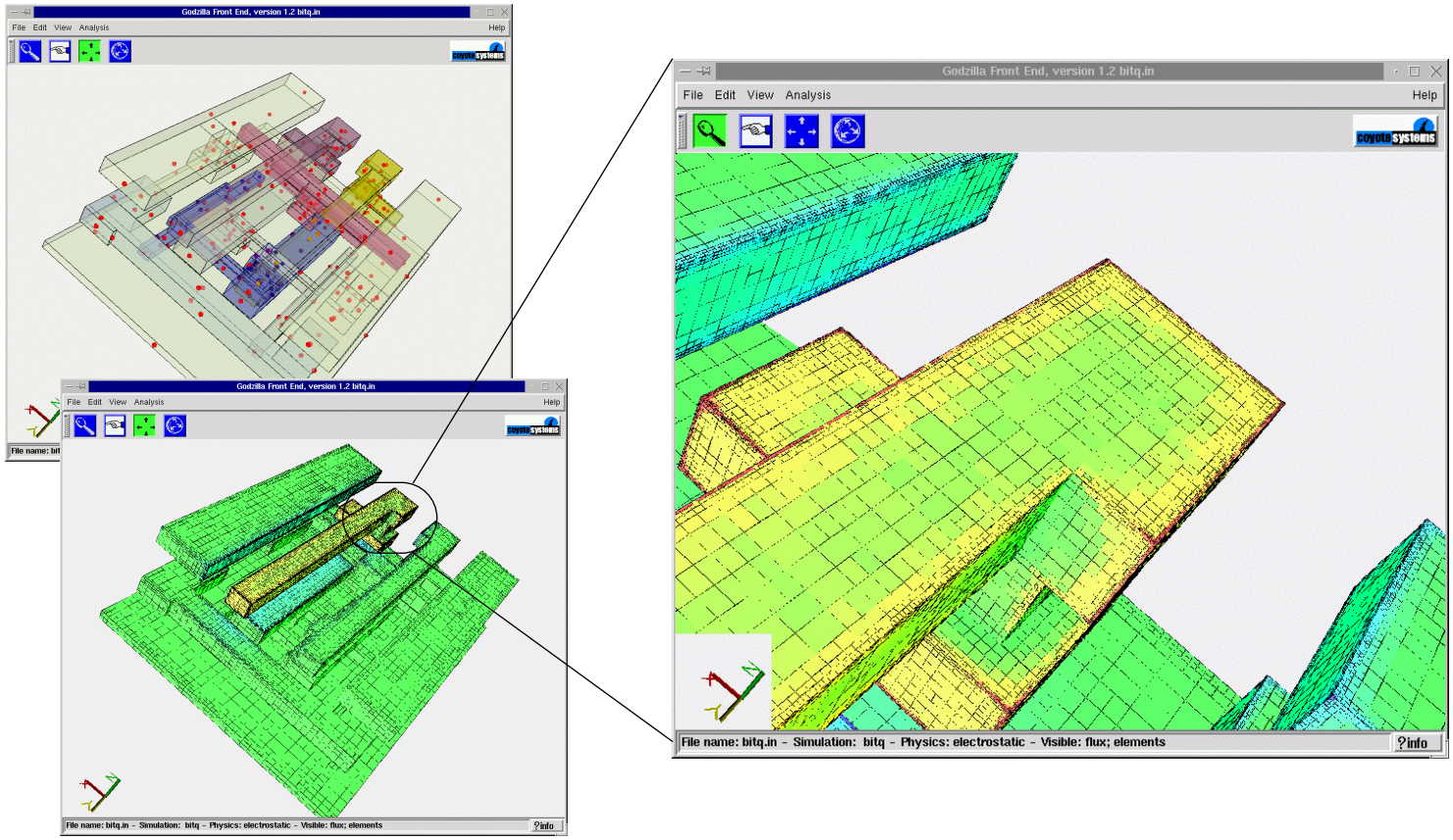
- **AutoIC simulates 10,000 cells in 2 hours**
  - **1 AutoIC license replaces 50-200 Raphael™ licenses**



  - **Adaptive meshing on SRAM bit-line shown**

Cell Optimization

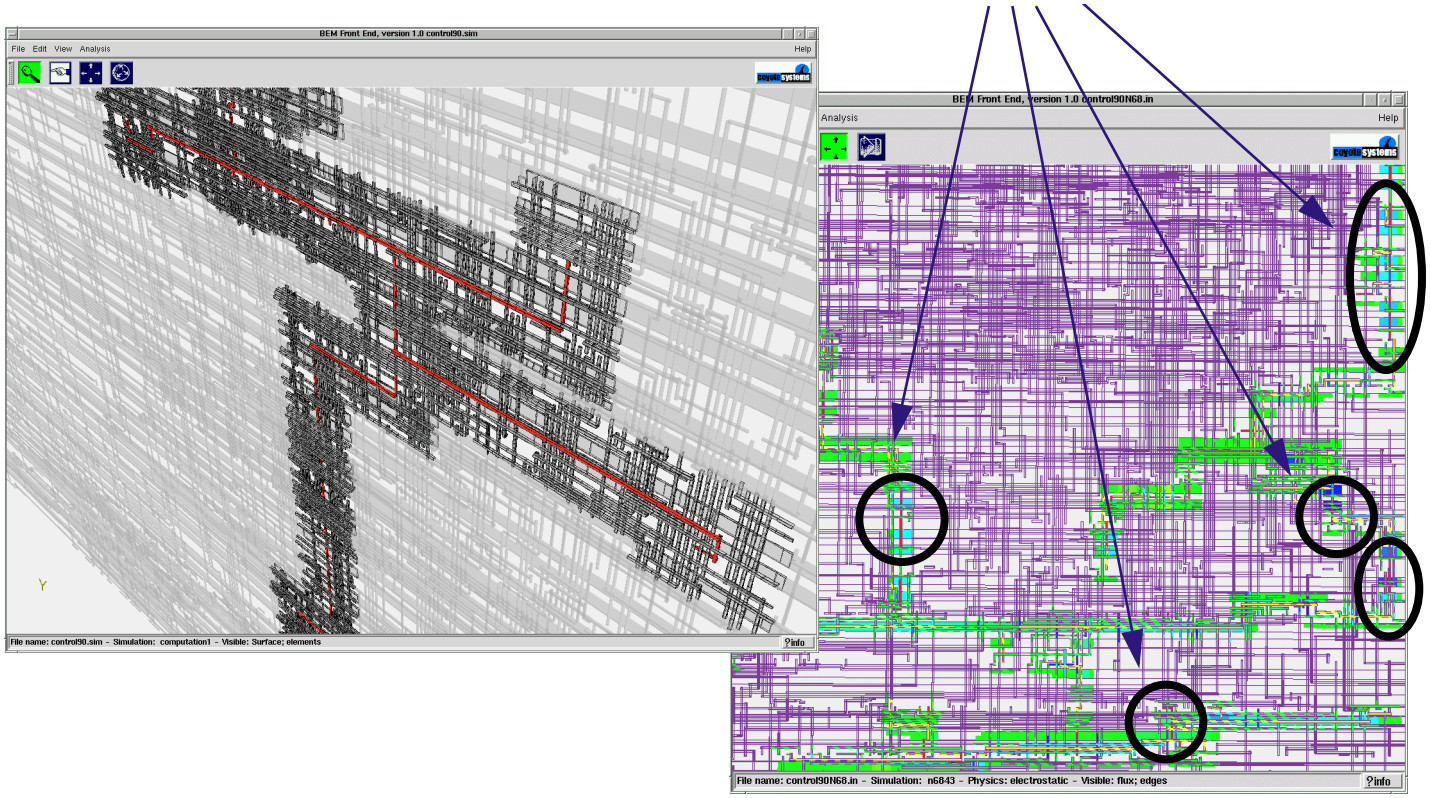
- AutoIC identifies where interactions occur
- Modify layout to optimize performance



- Magnitude of electrostatic flux on SRAM bit-line shown

Critical Nets

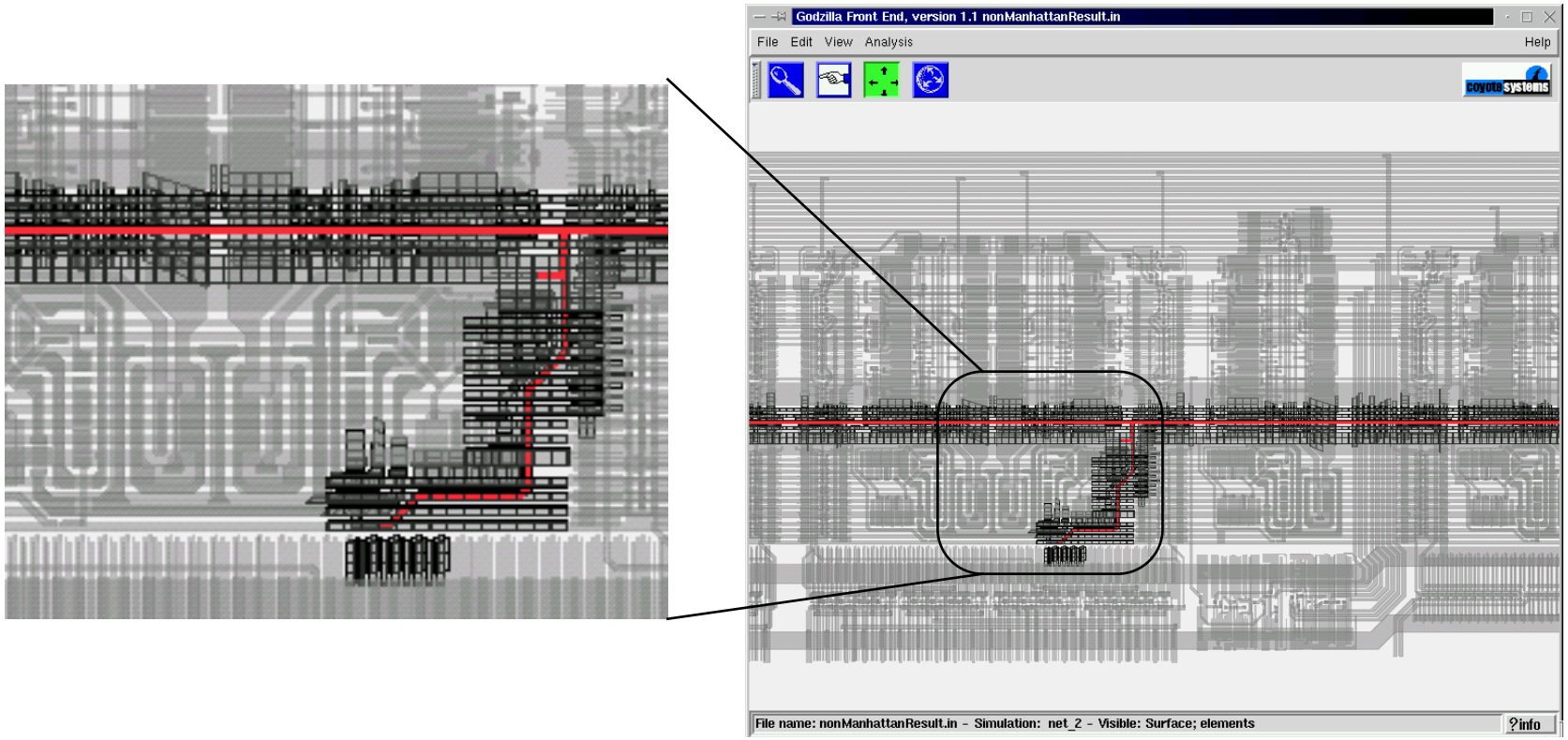
- **Handles largest global nets**
  - **Automatic tunneling around aggressor net**
  - **3D visualization indicates crosstalk areas**
  - **Designer can modify layout to eliminate problem**



- **1 AutoIC license replaces 10-50 QuickCap™ licenses**

Critical Blocks

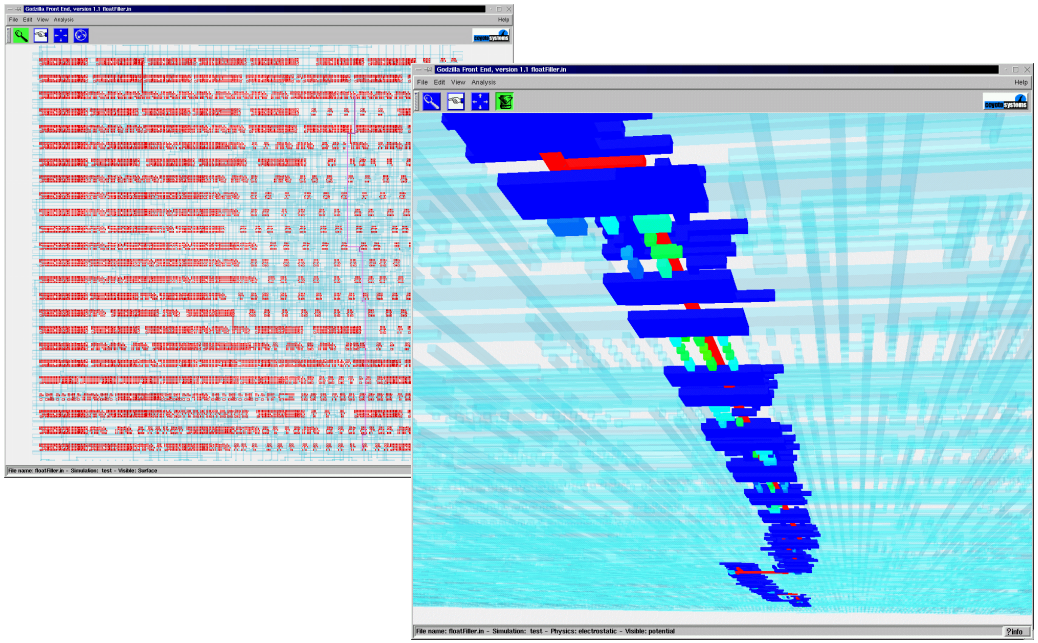
- PCB-style layout (Cypress)
  - Non-manhattan Geometries
  - Varying Linewidths
  - AutoIC 500x faster than QuickCap™!



- Aggressor net, 3D tunnel & 3D mesh shown

Non-Ideal Fabrication

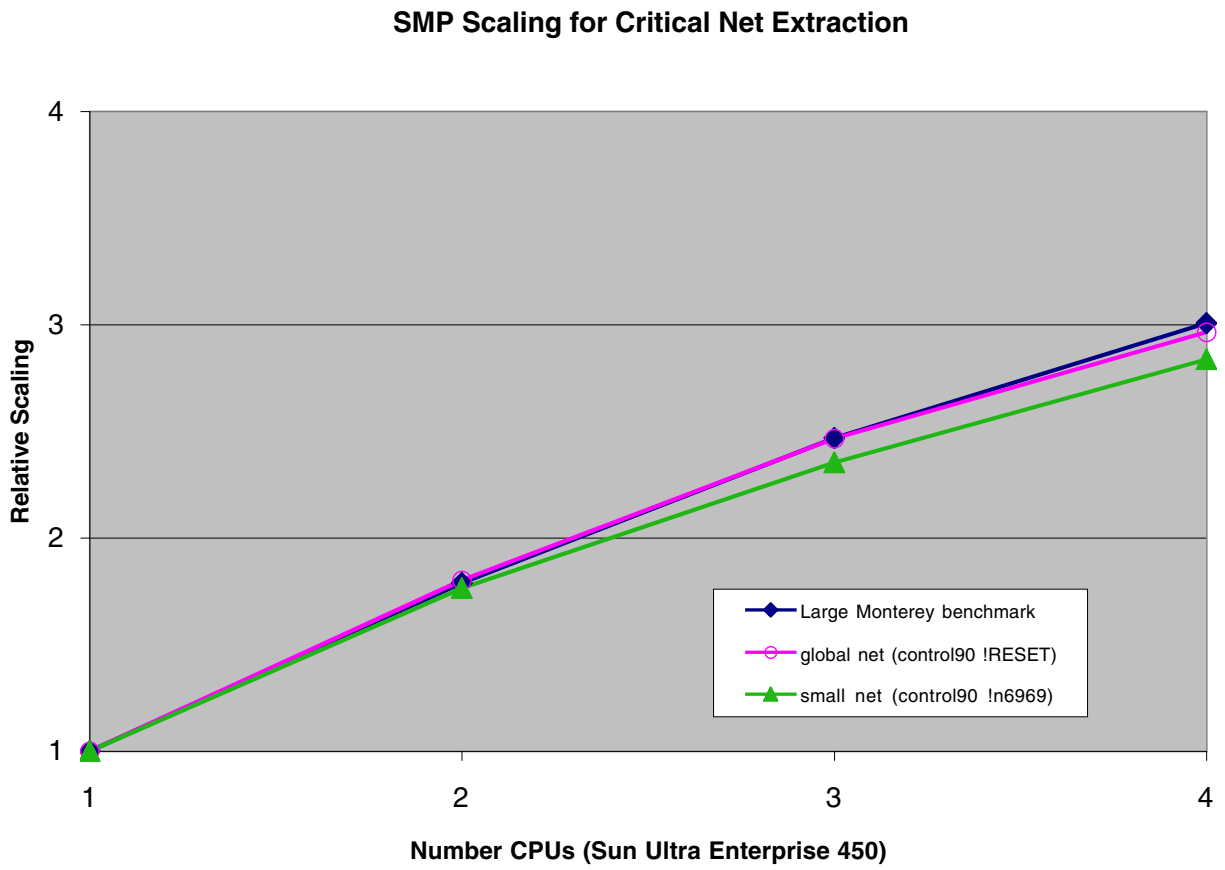
- AutoIC simulates Process Variations
  - Any geometry
  - Any material
- AutoIC correctly solves floating filler metal
  - Note that filler adds 20% to self-cap!



  - Non-zero potential on floating filler shown

AutoIC-SMP Scaling

- **Symmetric multiprocessing support**
  - **Excellent scaling with every added CPU**
  - **Accelerates both large and small nets**



"The Layout is the Design"

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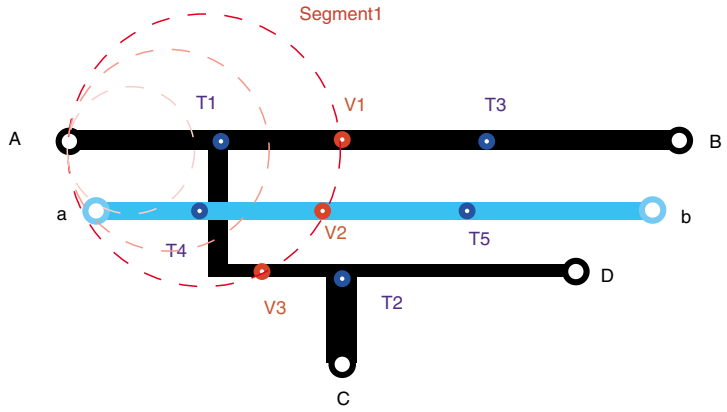
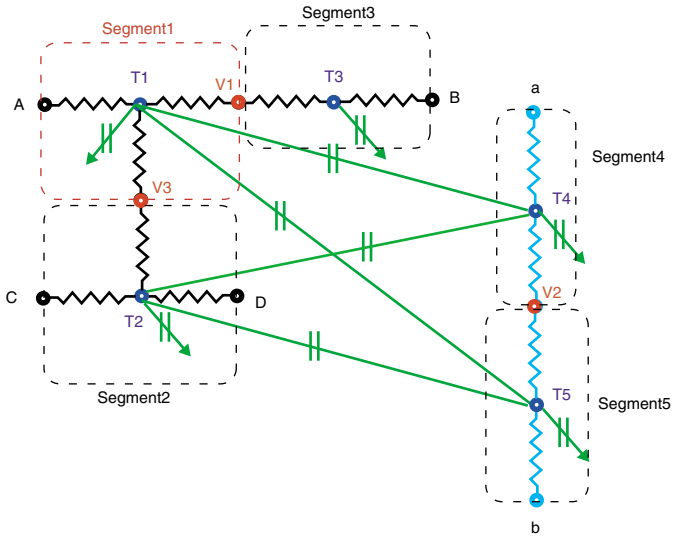
- **Timing Delay**
  - Self-capacitances dominate
- **Signal Integrity**
  - “Noise” or “Crosstalk”
  - Cross-capacitances dominate
- **AutoIC generates lumped RC models**
  - Extracts high-accuracy 3D self-caps and cross-caps from the interconnect layout
  - 3D visualization identifies areas for correction
- **AutoNet generates distributed RC models**
  - Important differences between lumped and distributed simulations

AutoNet

- Go from Layout to Distributed Spice
- Variable model size
  - Lumped net = 1 segment
  - Distributed net = multiple segments
- Segments
  - Spice star-model for each segment
  - Created from layout
  - Cross-caps between segments
  - Compact Spice model size
  - No model reduction needed





AutoNet

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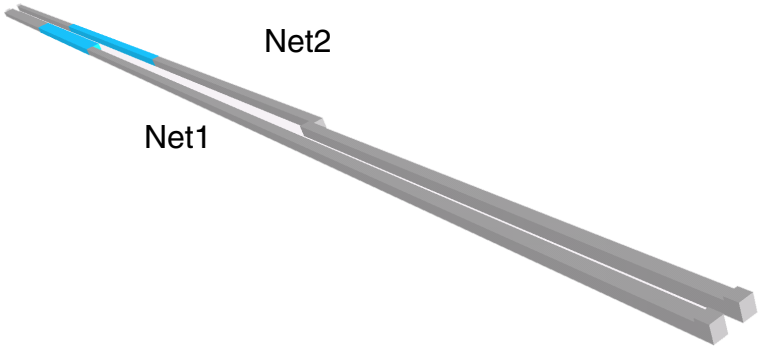
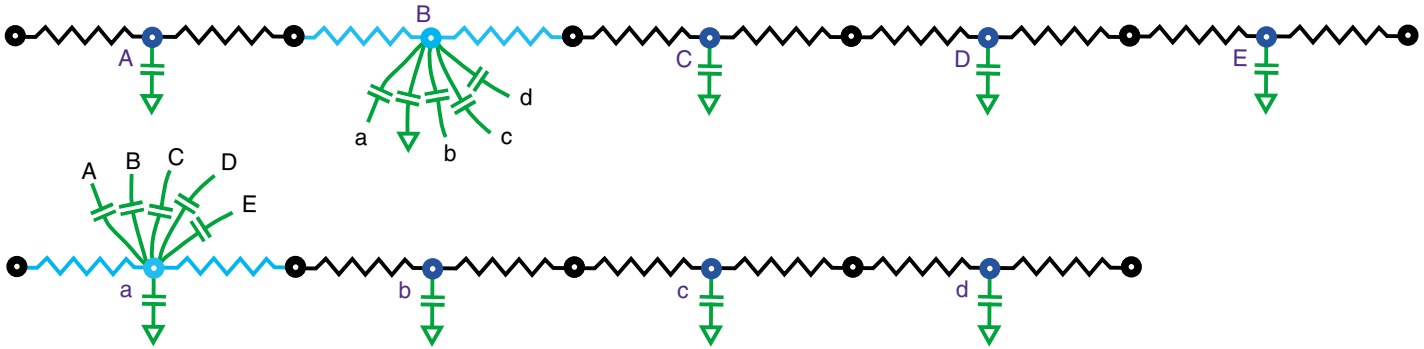
- **Automatic segmentation**
  - 5 segments on Net1
  - 4 segments on Net2



- **Distributed RC spice model**
  - Each segment has self-capacitance
  - Each segment has cross-capacitances to segments on other nets



AutoNet

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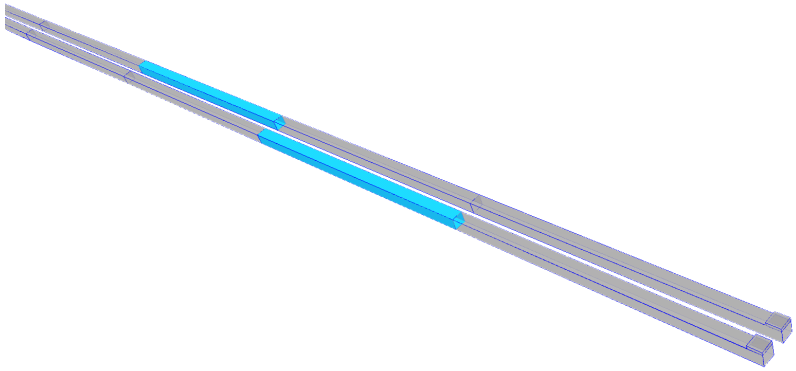
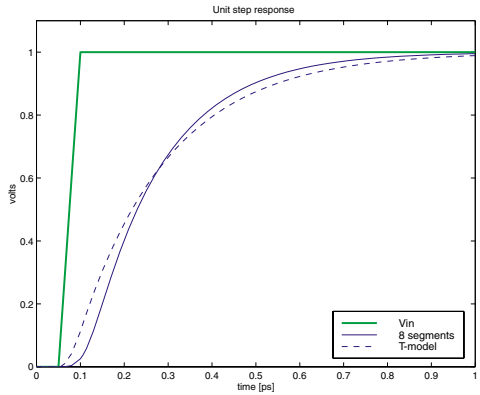
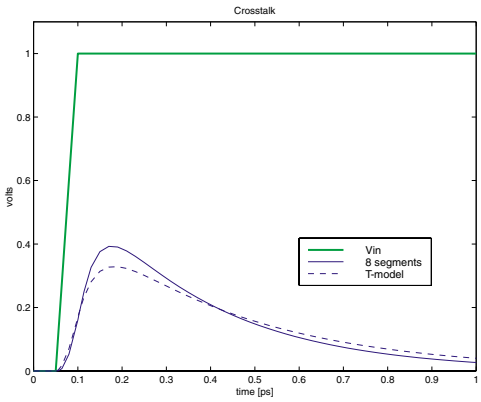
- **Parallel bus lines**
  - **Generated distributed model (8 segments per net)**
  - **Generated lumped T-model (1 segment per net)**







  - **Step Response**
    - Distributed and T model responses similar
  - **Coupling**
    - Distributed and lumped responses similar

AutoNet

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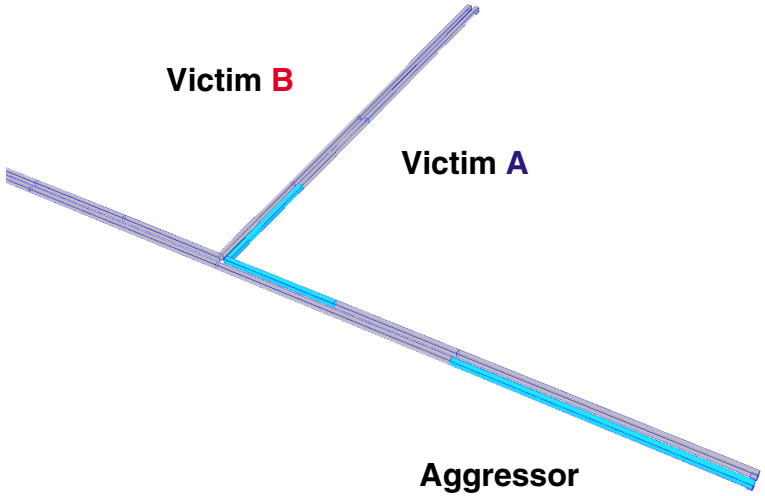
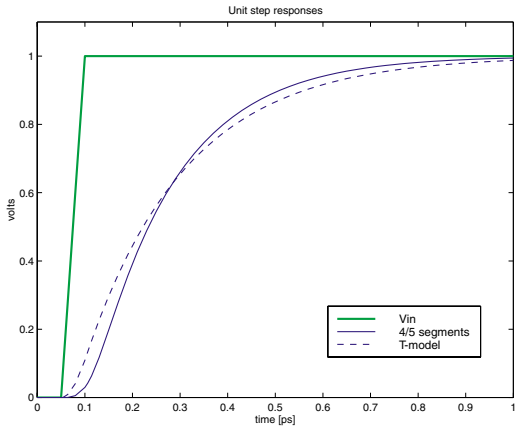
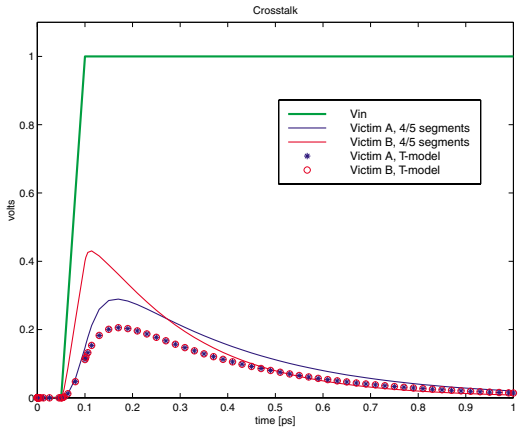
- **Non-uniform bus lines**
  - **Generated distributed model (4-5 segments per net)**
  - **Generated lumped T-model (1 segment per net)**







  - **Step Response**
    - Distributed and T model responses similar
  - **Coupling**
    - 2x more noise on distributed model

AutoNet

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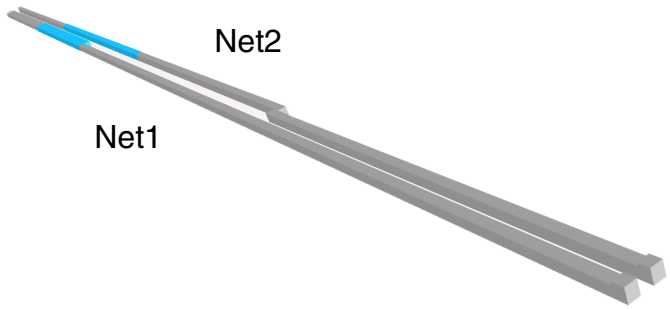
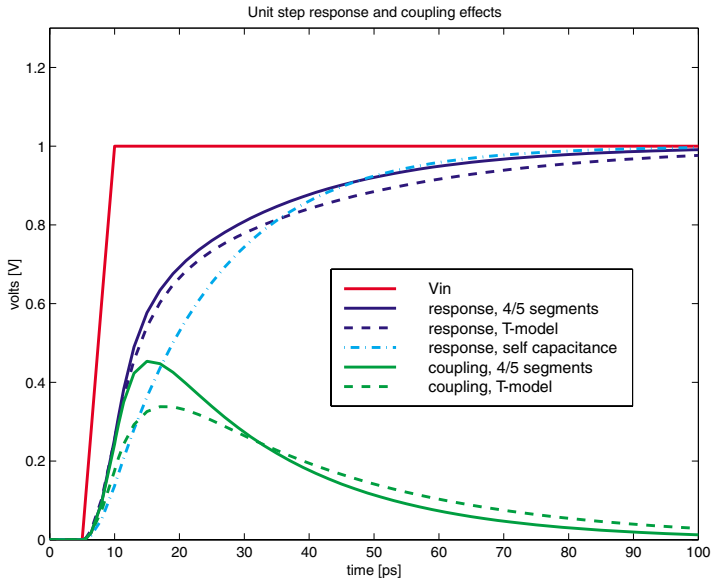
- **Parallel lines with varying cross-section**
  - **Net1 switches**





  - **Step Response**
    - Distributed and T models similar
    - Commonly used self-cap model is inaccurate
  - **Coupling**
    - 30% larger noise with distributed model

AutoNet

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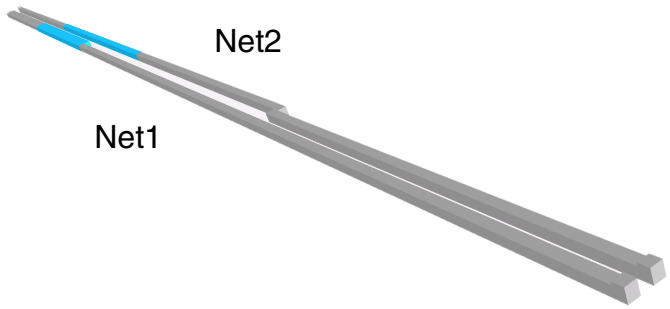
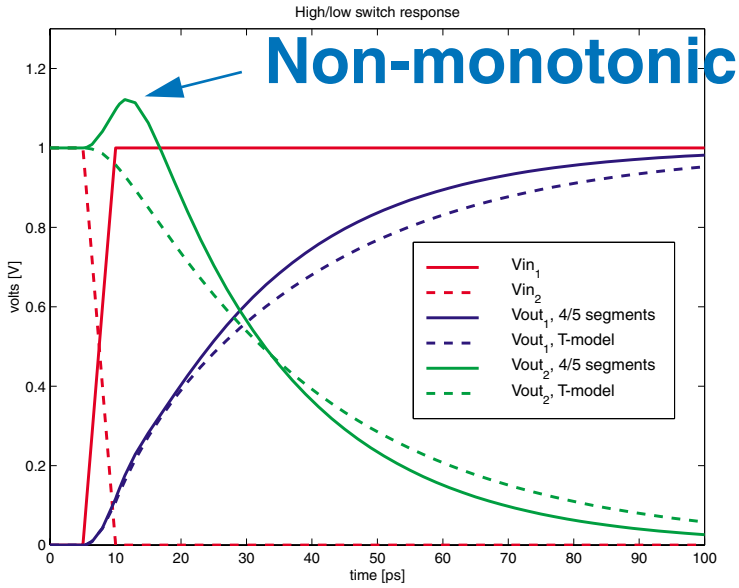
Non-uniform parallel lines

- **Nets switch in opposite directions**

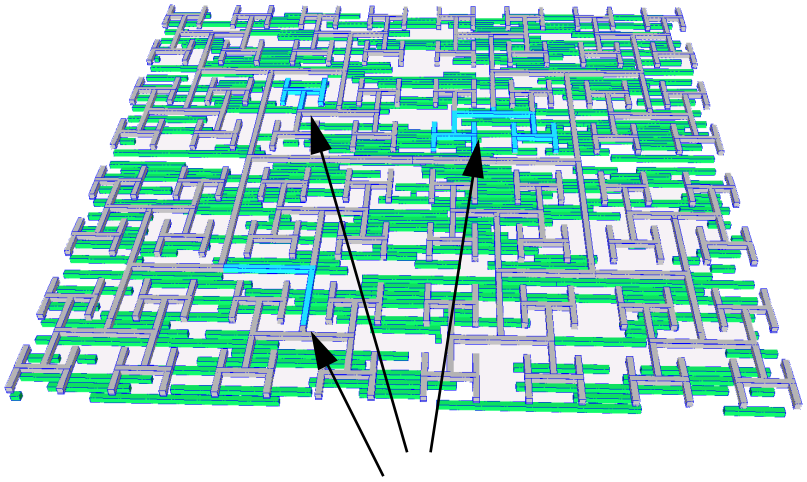




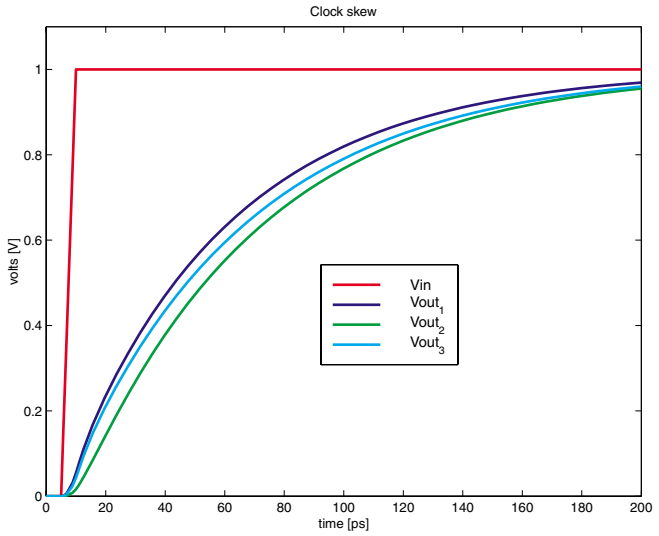
- **Step Response**
  - Distributed and T models similar
- **Coupling**
  - Distributed model shows non-monotonic behavior

Clock Tree Skew

- Hierarchical H-shaped layout
- 256 terminals



sample segments

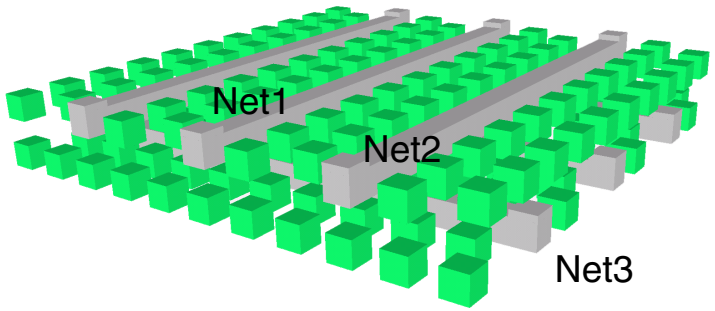


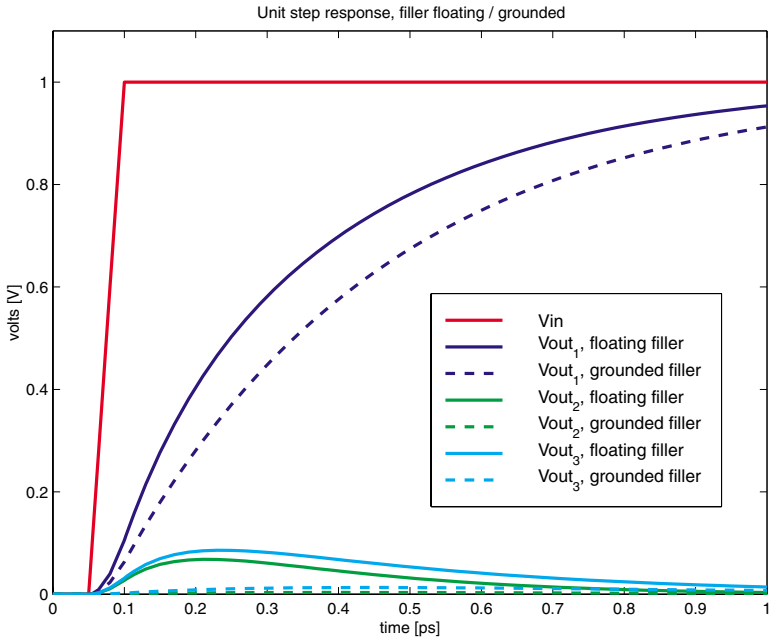
- RC model with 70 segments
- Non-constant clock skew due to cross capacitances
- 20% clock skew at 3 random clock terminals!

AutoNet

coyotesystems

- **Compare Floating Filler & Grounded Filler**
  - **3x3 crossing bus**
  - **Net1 switches**

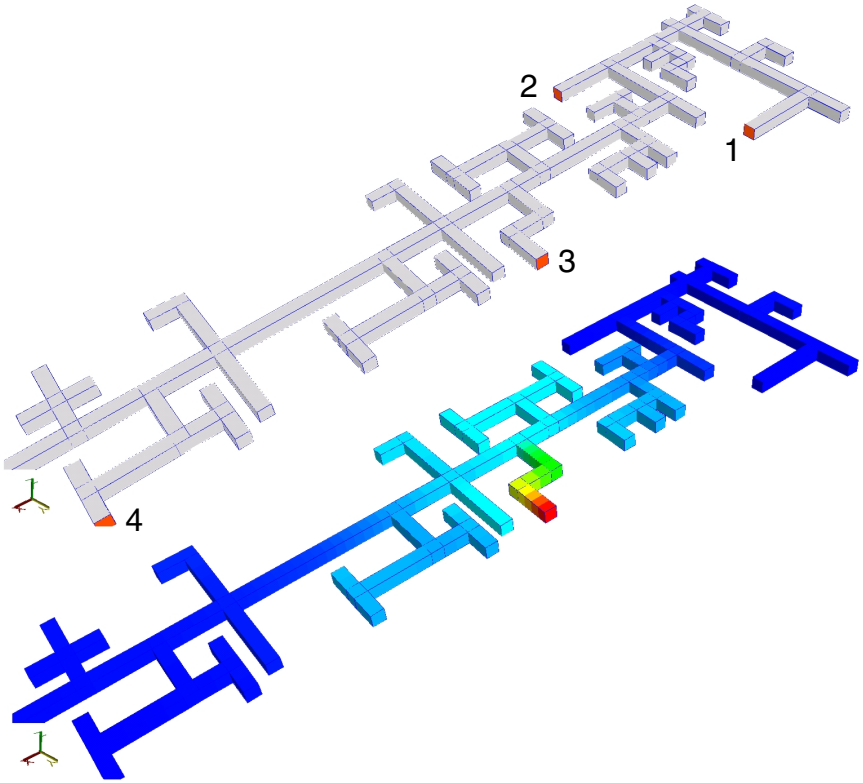




- **Significant filler problem**
  - **25% difference in risetime**
  - **9x increase in noise level**

AutoIRdrop

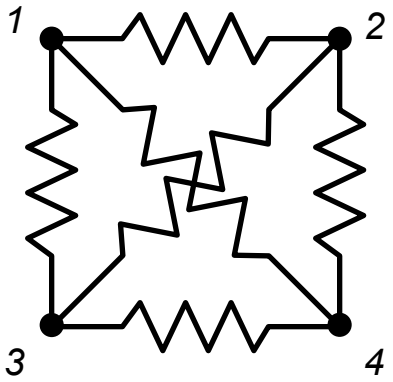
- **AutoIC solves 3D field outside interconnects**
- **AutoIRdrop solves 2D/3D field inside interconnects**
  - **Varying angles, width, cross-section**
  - **Vias**
  - **Aluminum, copper**
  - **Current sink/source**
- **2D/3D Field Solver**
  - **Solves potential drop**
    - Resistance
  - **Solves current density through wire**
    - Enables electromigration analysis



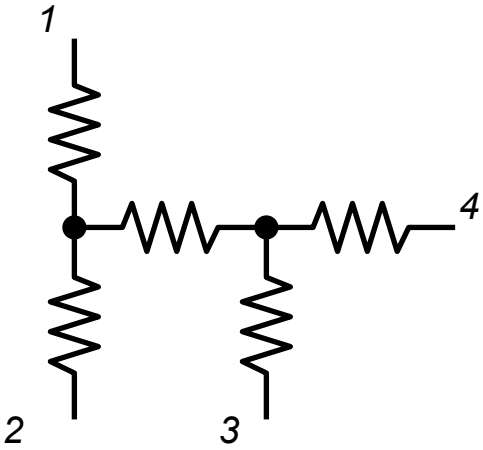
AutoIRdrop

coyote systems

- "Naive" Resistance Network
  - N-ports require N simulations, resulting in N^2 resistances



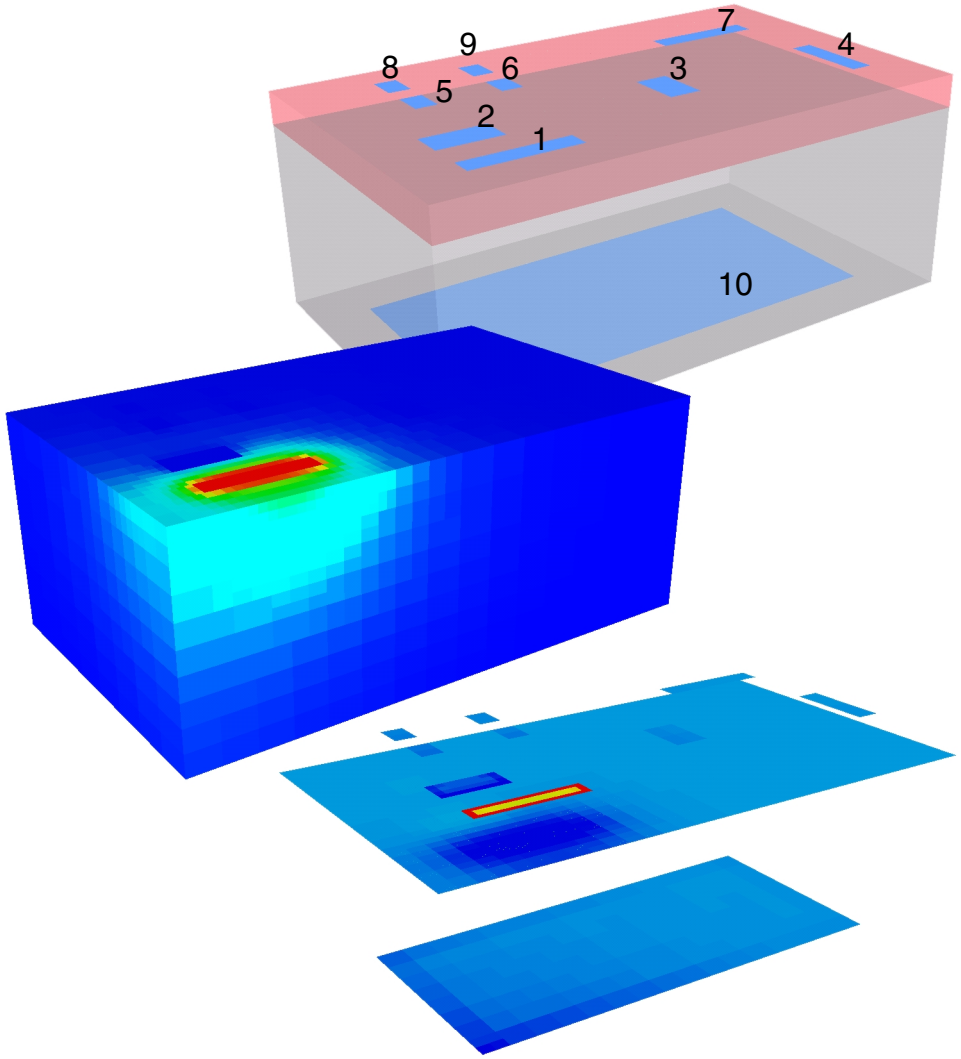
- "Smart" Resistance Network
  - N-ports require N simulations, resulting in N resistances



- Field Simulation
  - 2D resistance is very accurate, much faster than 3D
  - 2D suitable for resistance, 3D suitable for capacitance

AutoSubstrate

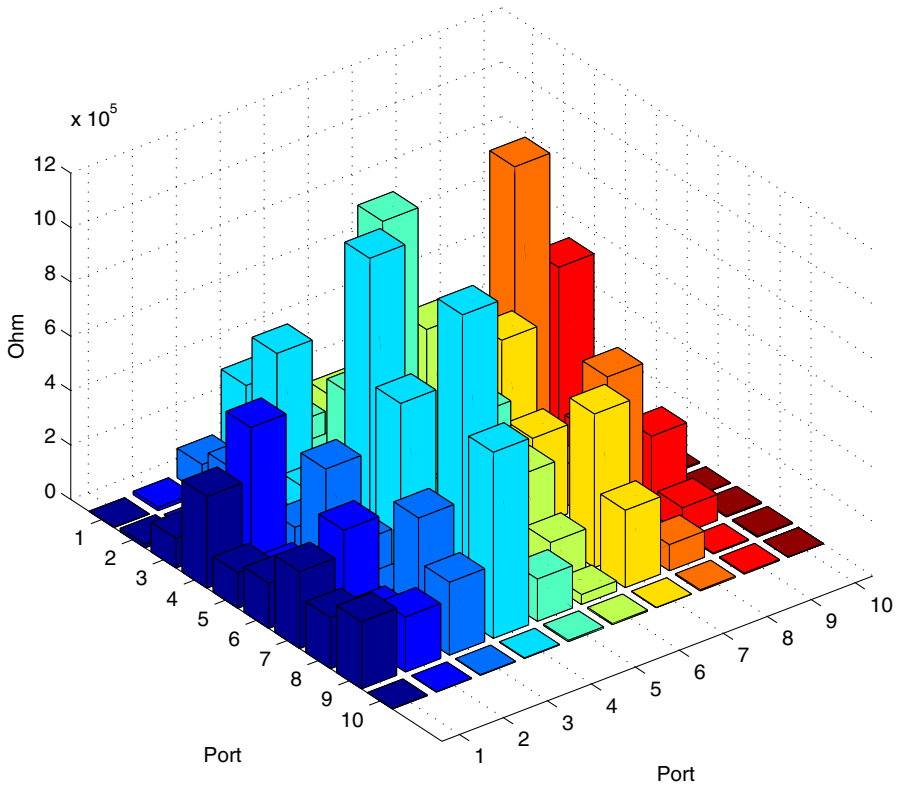
- **Solves 3D field inside substrates**
  - Contacts
  - Multiple materials
- **3D Field Solver**
  - Solves potential distribution
  - Solves electrostatic flux distribution
  - Solves current density through contacts



AutoSubstrate

coyotesystems

- **Resistance Network**
  - Resistance calculated from calculated current densities
  - Resistor for every port-port interaction
  - Automatic spice model



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