BSIM4 MOSFET Model for Circuit Simulation

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Acknowledgement

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- BSIM team: Dr. Weidong Liu, Xiaodong Jin, Mark Cao, Jeff Ou

Berkeley Short-channel IGFET Model (BSIM) - Industry Standard Model

- BSIM3v3 has been chosen as the first industry standard model for circuit simulation and is supported by EIA Compact Model Council (CMC), a consortium of 20 companies including IBM, Intel, TI, Motorola, Lucent, AMD, Hitachi, Philips, Infineon, TSMC, Cadence, Avanti, etc.

- As a standard model, BSIM simplifies technology sharing, foundry and other partnerships, and improves productivity.

Review of BSIM3

BSIM3 Accounts for Major Physical Mechanisms

- Short/Narrow Channel Effects on Threshold Voltage
- Non-Uniform Doping Effects
- Mobility Reduction Due to Vertical Field
- Bulk Charge Effect
- Carrier Velocity Saturation
- Drain Induced Barrier Lowering (DIBL)
- Channel Length Modulation (CLM)
- Substrate Current Induced Body Effect (SCBE)
- Parasitic Resistance Effects
- Quantum Mechanic Charge Thickness Model
- Unified Flicker Noise Model

BSIM4 Overview

Basic IV model

Vth **model for pocket/retrograde technologies**

Vgsteff

Bulk charge (*Abulk*) model

Mobility models

Rout **model**

GIDL current model

Bias-dependent *Rds*(V) model, internal or external

Gate (equivalent) *Tox* and dielectric constant, and quantum-mechanical charge-layer thickness model

BSIM4 Overview

RF and High-speed model

- Intrinsic input resistance (*Rii*) model
- Non-Quasi-Static (NQS) model
- Holistic and noise-partition thermal noise model
- Substrate resistance network

Flicker noise model

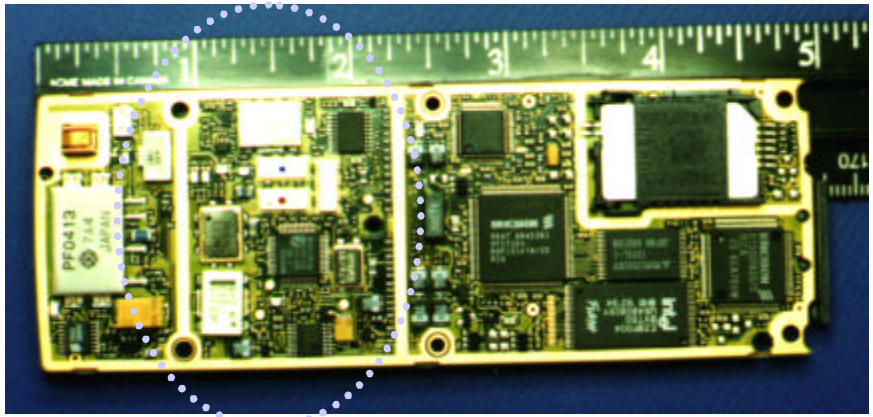
Geometry calculation (Layout-dependent parasitics) model

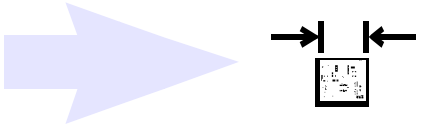
Asymmetrical source/drain junction diode model

- I-V and breakdown model

Gate dielectric tunneling current model

Put Radio On A Single Chip





ISSCC'97

- **The ultimate goal: integrate the whole system on a chip (SOC)**
- **Advantages: lower cost, smaller form factor, better performance**

State-of-the-art RF Model Is Table Lookup

- **Table lookup model is not a good solution.**

Table Lookup vs. Compact Model

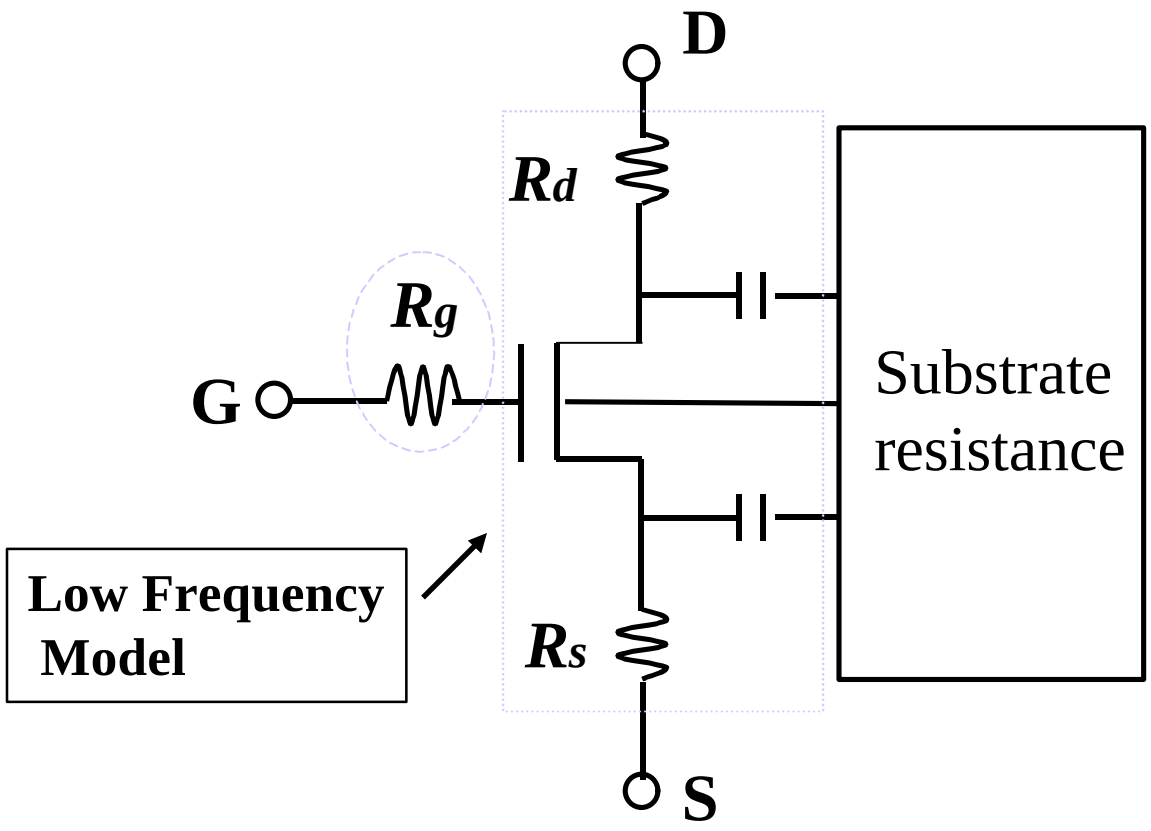
	Accuracy at RF	SOC simulation	Efficiency	Scalability	Predictive ability
Table lookup	+	-	-	-	-
Compact Model	Present model is inadequate	+	+	+	+

Missing Pieces

What are missing in the low frequency models:

- Intrinsic input resistance which is function of channel length and bias
- Thermal noise becomes very important in RF circuits for communications. The 20-year old long channel thermal noise model is not acceptable any more.
- Extrinsic resistance: gate electrode resistance and substrate resistance

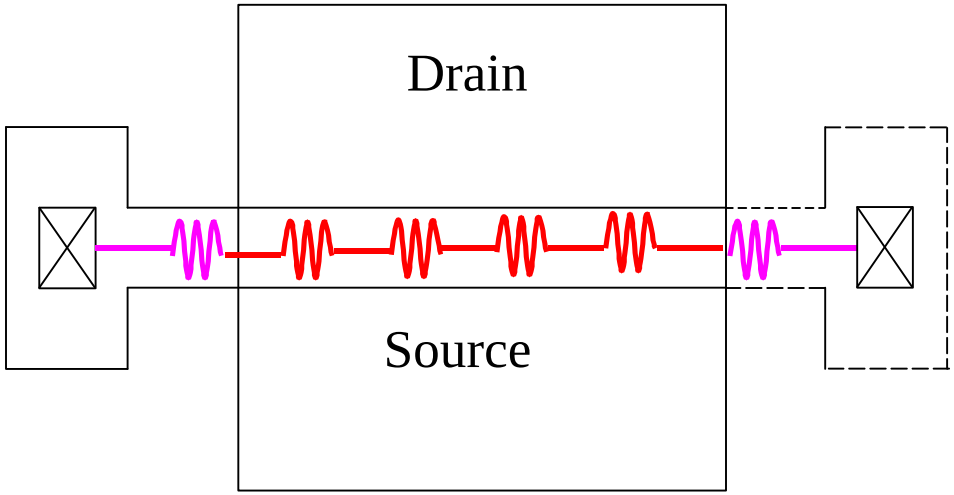
BSIM4 RF Model



RF model requires accurate low frequency model, Rg and Rsub

Electrode Resistance is A Minor Part of Gate Resistance

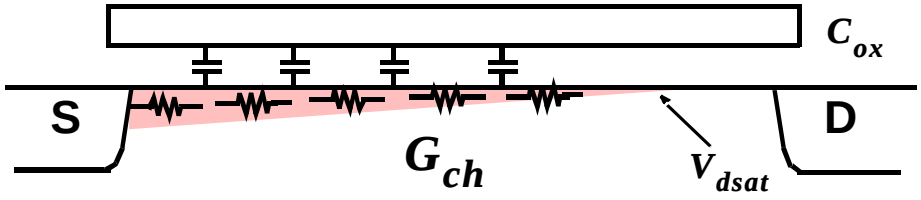
Gate electrode resistance:



It is independent of bias, decreases as L increases

Most of Gate Resistance Is Intrinsic

Intrinsic input resistance:



$$R_{ii} \propto R_{ch} = \frac{1}{G_{ch}}$$

The proportion constant is determined by 2-D simulation ~14

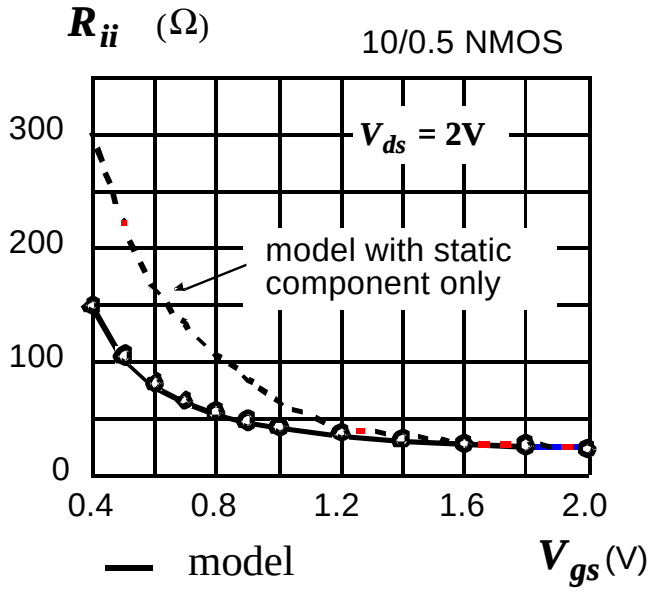
$$G_{ch} = G_{st} + G_{ed}$$

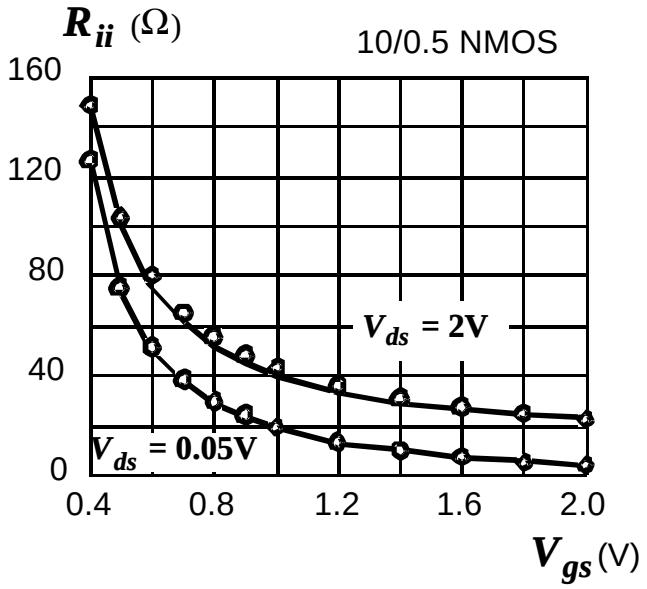
$$G_{st} = \frac{1}{\int dR} = \frac{I_d}{\int dV} = I_d / V_{dsat} \quad \text{in saturation}$$

$$= I_{ds} / V_{ds} \quad \text{in triode}$$

$$G_{ed} = \frac{kT}{q} m_{eff} C_{ox} \frac{W}{L}$$

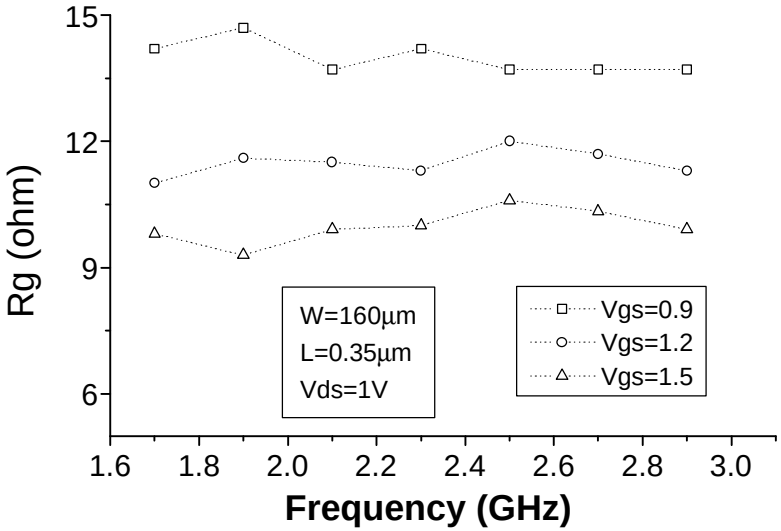
2-D Simulation Verification of Rii Model

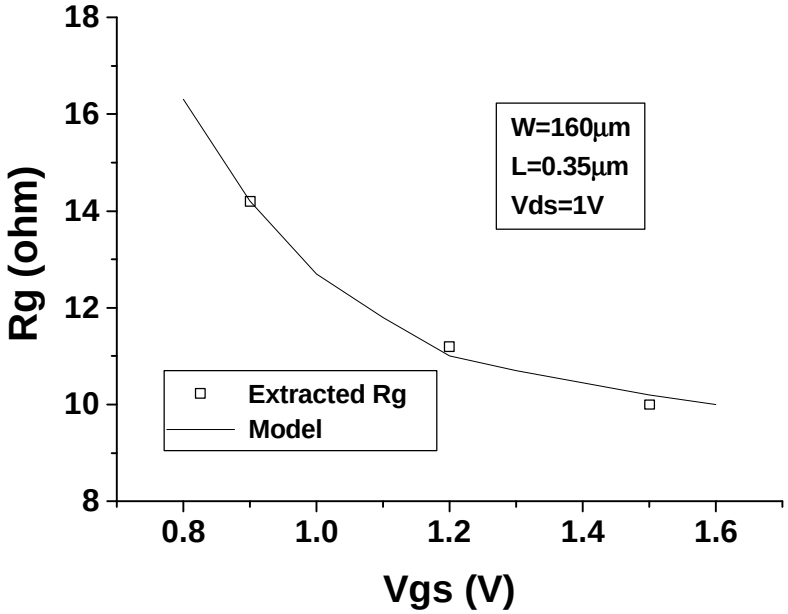




- **2-D simulation shows a non-zero Rii**
- **A single analytical function models dependency of Rii on Vds, Vgs and L**

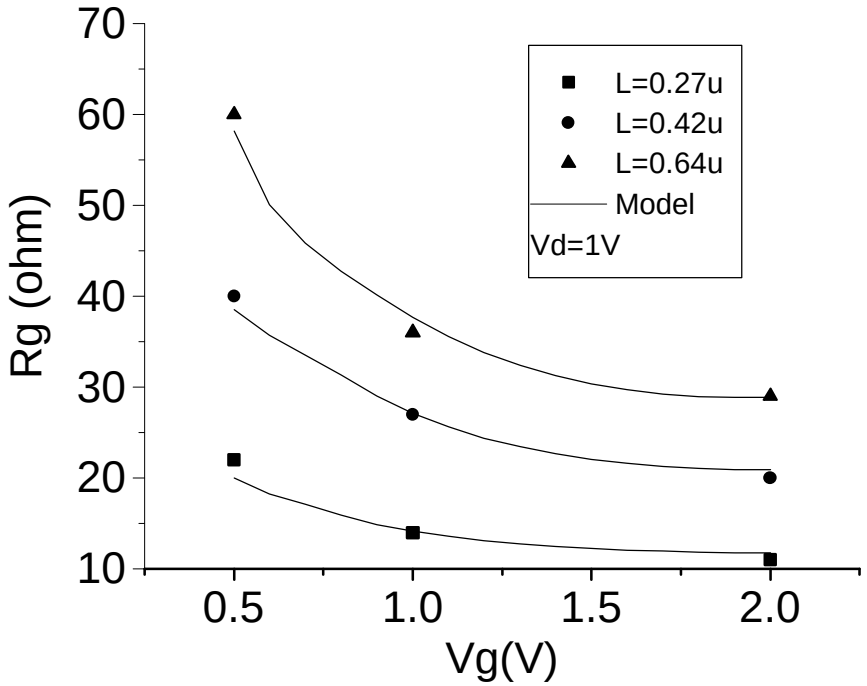
Measurement Verification of Rii Model





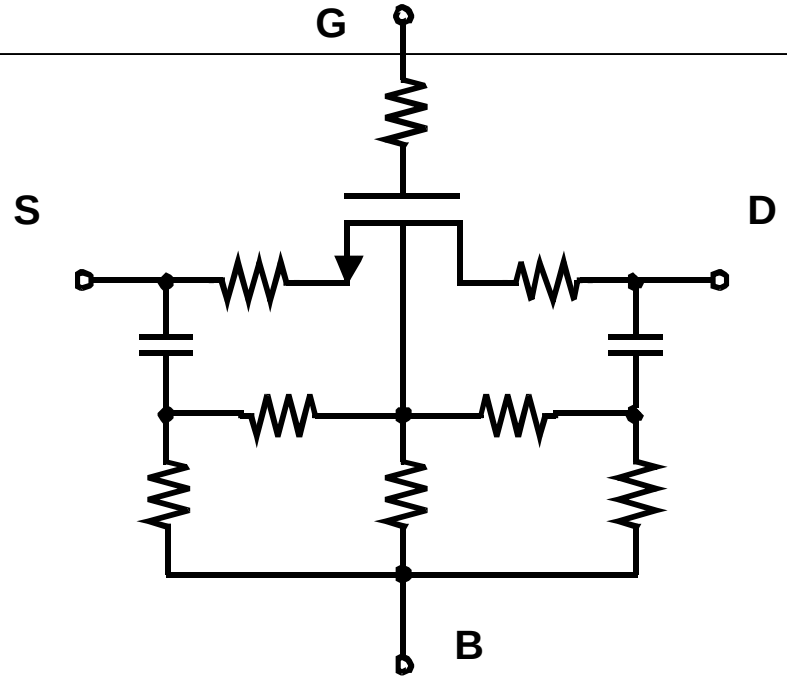
- **Measured data show Rg is independent of frequency**
- **Rg is strong function of bias**

Verification of Rii With Different L



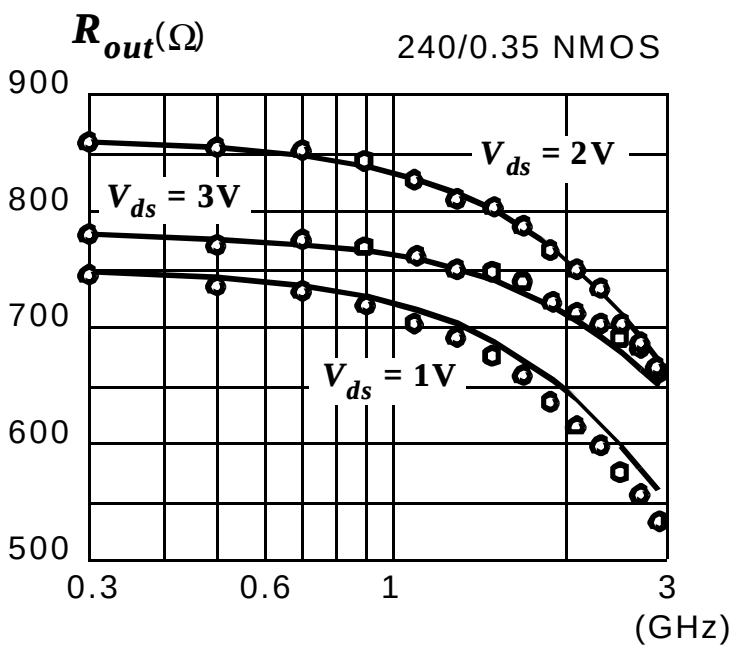
- Measurements show Rg increases as L increases
- The intrinsic input resistance is dominant over gate electrode resistance

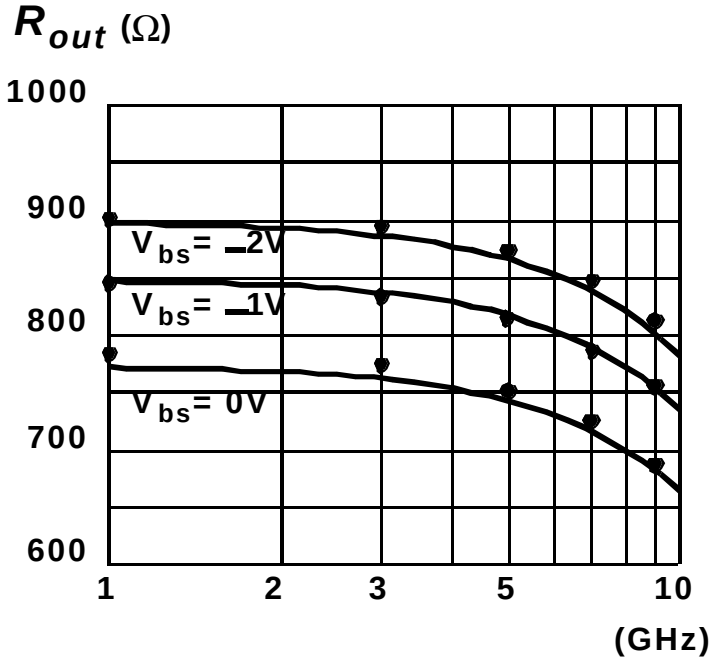
Substrate Network



- **Substrate resistance is responsible for the Rout roll-off at high frequency**
- **In practice, two or three resistors are sufficient for accurate modeling**
- **BSIM4 allows user to use 0-5 resistors**

Substrate Network Model Verification





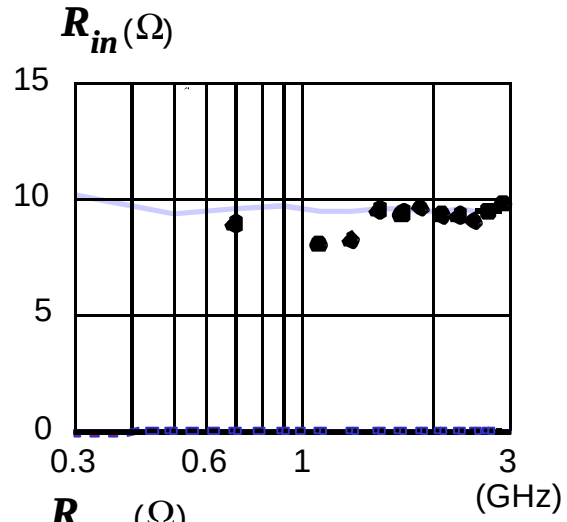
○ : measurement

● :2-D simulation

— : BSIM RF

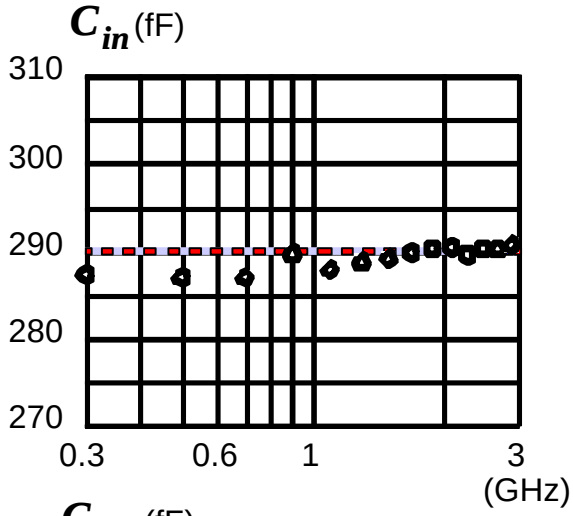
Two substrate resistors can fit the Rout for different Vds or Vbs

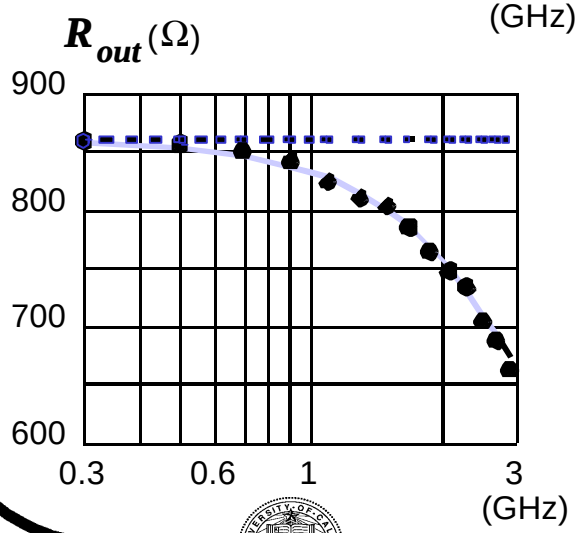
Measurement Verification of BSIM4 RF Model



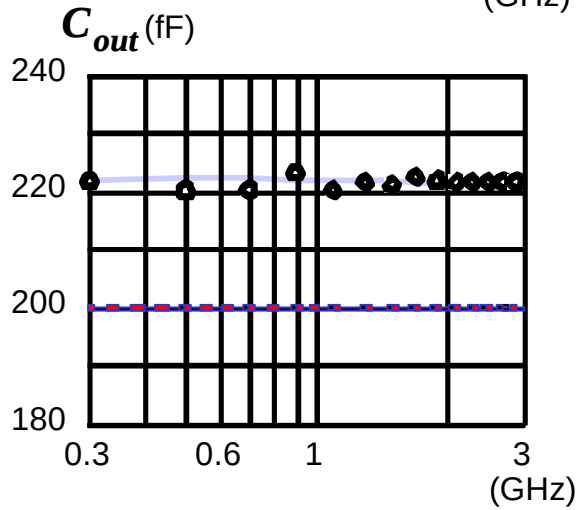
Measured
BSIM3v3
BSIM RF

Rg = 9.5 Ω
$R_{Subd,s}$ = 50 Ω

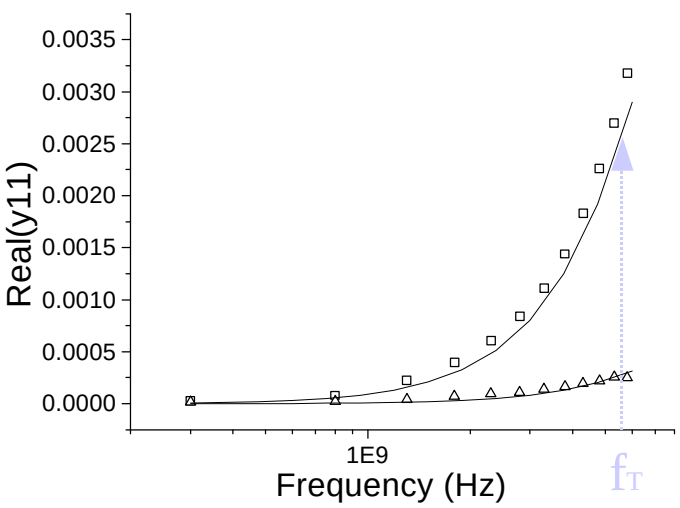


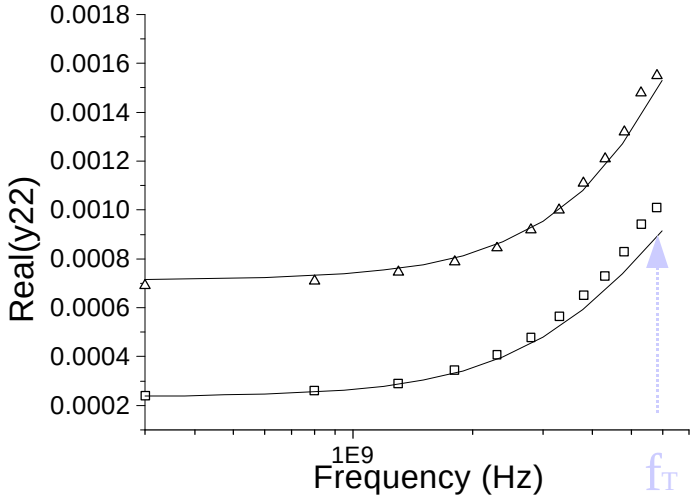


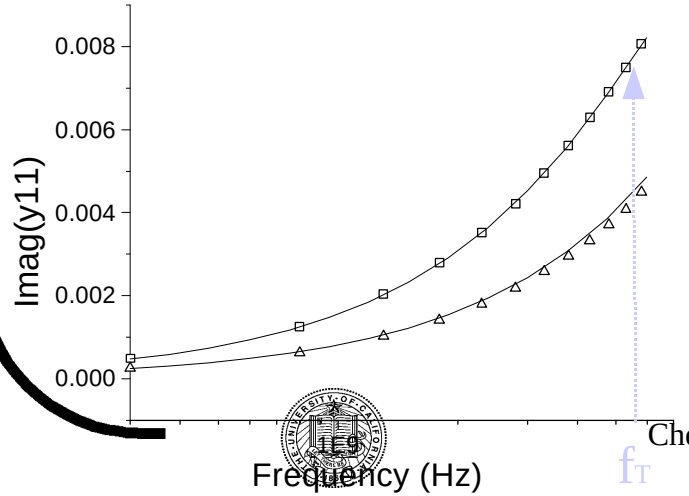
24-finger
240/0.35 NMOS
V_{gs} = 0.9 V V_{ds} = 2 V

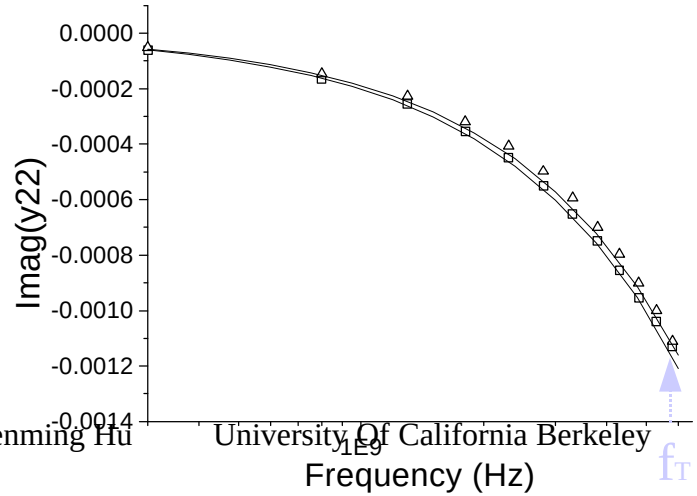


Verification of Scalability of RF Model









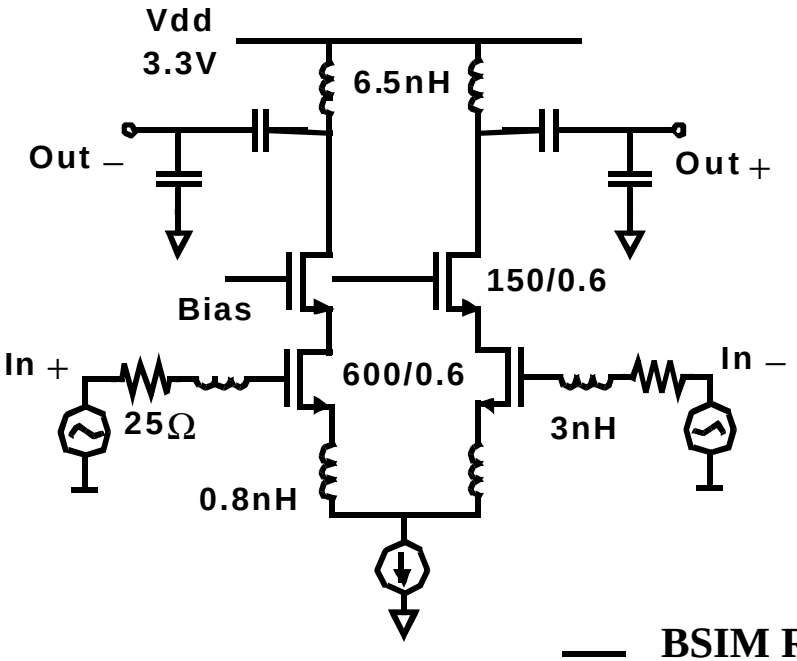
— model

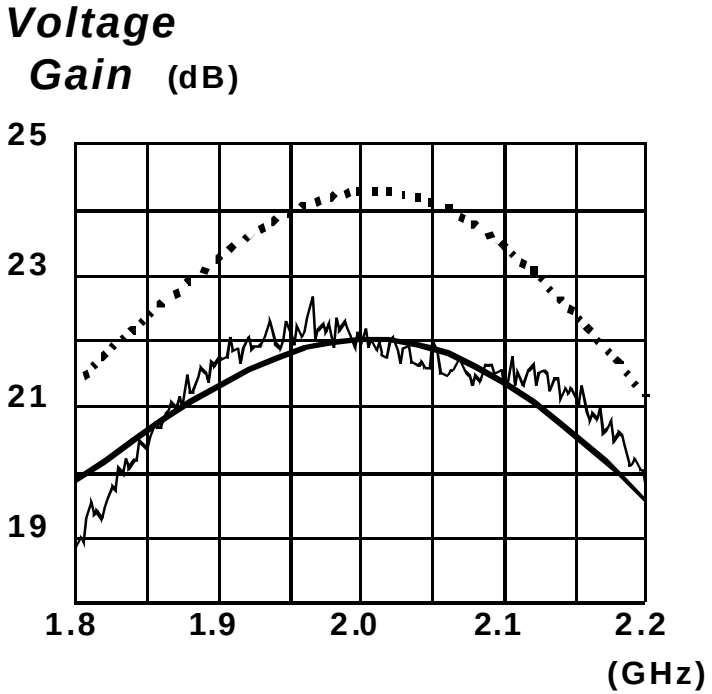
Δ L=0.27um
f_T=14GHz

□ L=0.64um
f_T=6GHz

Vgs=Vds=1V

Circuit Level Verification of RF Model





- A prototype LNA was fabricated in 0.6um CMOS
- Measured result confirms the BSIM RF model

Holistic Thermal Noise Model

Holistic Thermal Noise Model

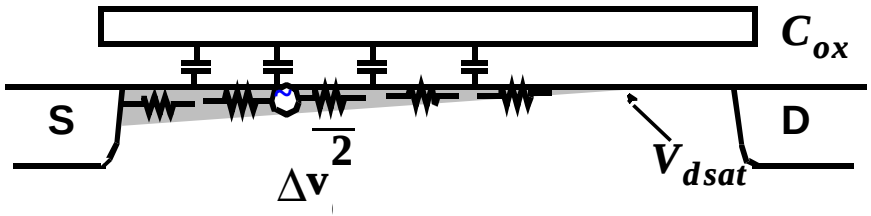
Channel Thermal Noise Model

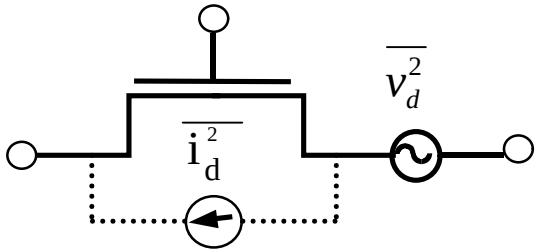
-- physical, all short channel and other effect in the BSIM DC model automatically included in noise.
-- Gate amplification of noise dominates channel resistance noise

Noise-Partition Model

-- Unifies the induced gate noise and channel noise with correlation

Holistic Thermal Noise Model





$$\overline{v_d^2} = \int \overline{\Delta v_d^2} = 4kTB \int dR$$

$$= 4kTB \frac{V_d}{I_d}$$

$$\overline{i_d^2} = \overline{v_d^2} g_{ds}^2$$

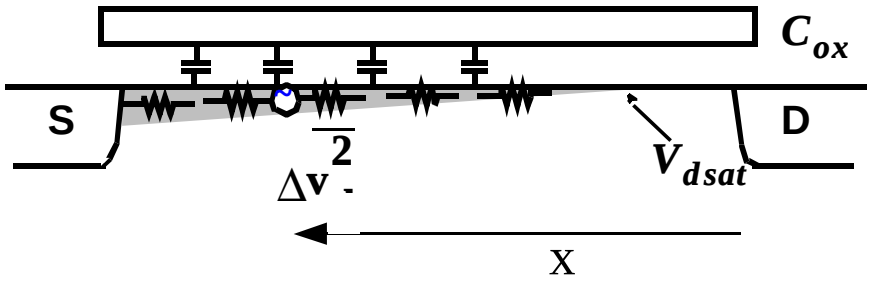
$$= 4kTB \frac{V_d}{I_d} g_{ds}^2$$

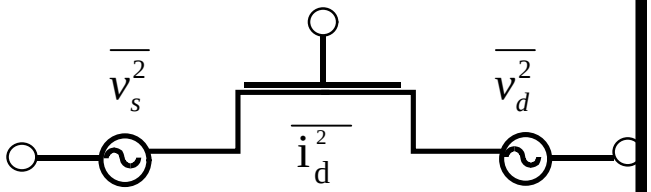
$$\frac{V_d}{I_d} \equiv \frac{V_{dsat}}{I_{ds}} \quad \text{in saturation}$$

$$\equiv \frac{V_{ds}}{I_{ds}} \quad \text{in triode}$$

Channel Noise

Amplification by Gate and Back-gate





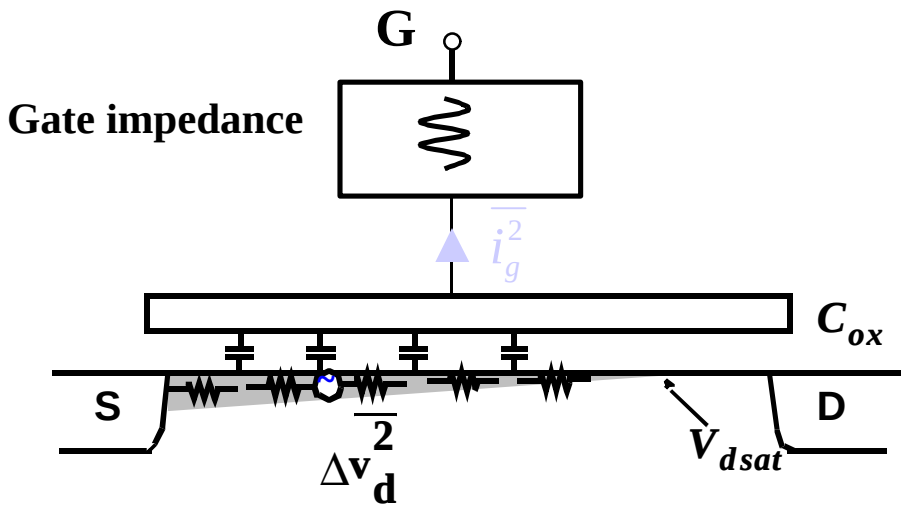
$$\Delta i_d = \Delta v(g_{ds} + g_{mx} + g_{mbx})$$

$$\overline{i_d^2} = \overline{v_d^2}(bg_m + bg_{mb} + g_{ds})^2$$

$$= 4kTB\frac{V_d}{I_d}(bg_m + bg_{mb} + g_{ds})^2$$

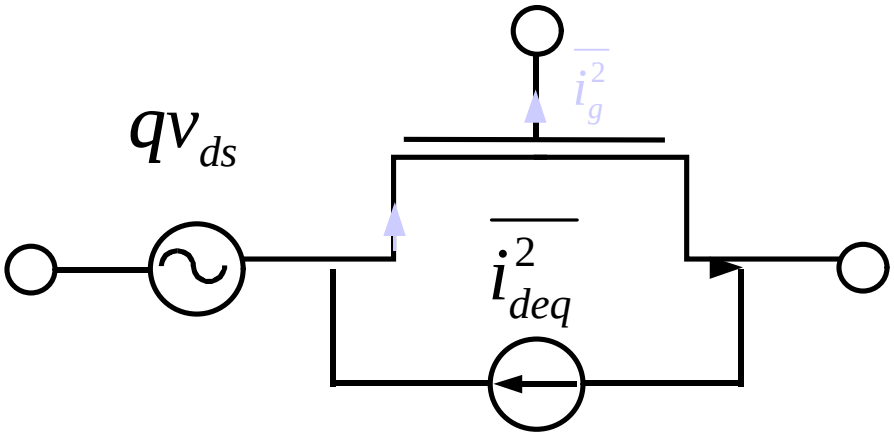
- **Channel resistance noise is amplified by the gate and back-gate**

Unified Model of Channel Noise and Induced Gate Noise



- **At high frequencies, the elemental channel resistance noise source will generate significant noise current through the gate capacitance.**
- **The induced gate noise is correlated with the channel noise**

Noise Partition Model

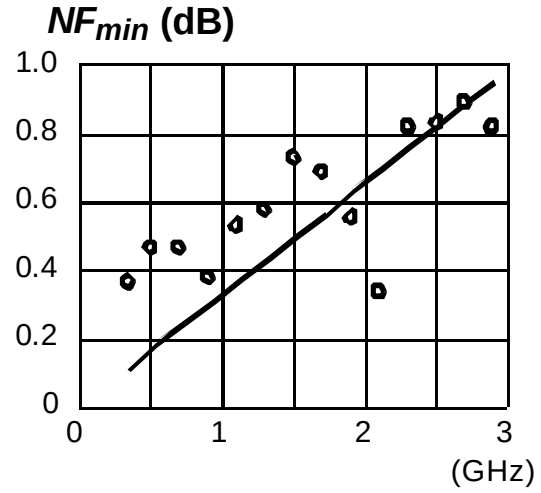


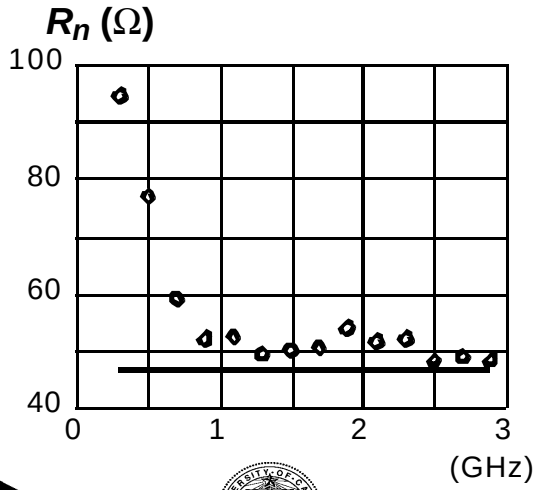
$$\overline{v_d^2} = 4kTB\frac{V_d}{I_d}$$

$$\overline{i_{d,new}^2} = \overline{i_d^2} - 4kTBq^2(g_m + g_{mb} + g_{ds})^2(\frac{V_d}{I_d})$$

The total noise can be partitioned into two parts to model induced gate noise

Measurement Verification of Holistic Noise Model

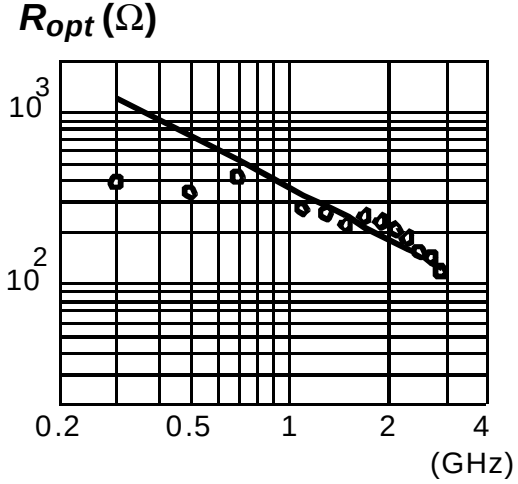


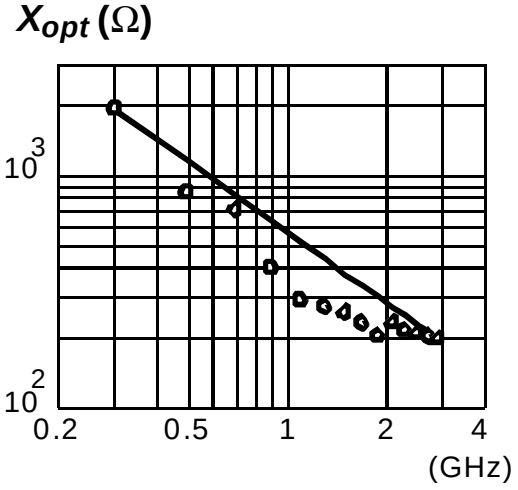


o measurement
— BSIM RF

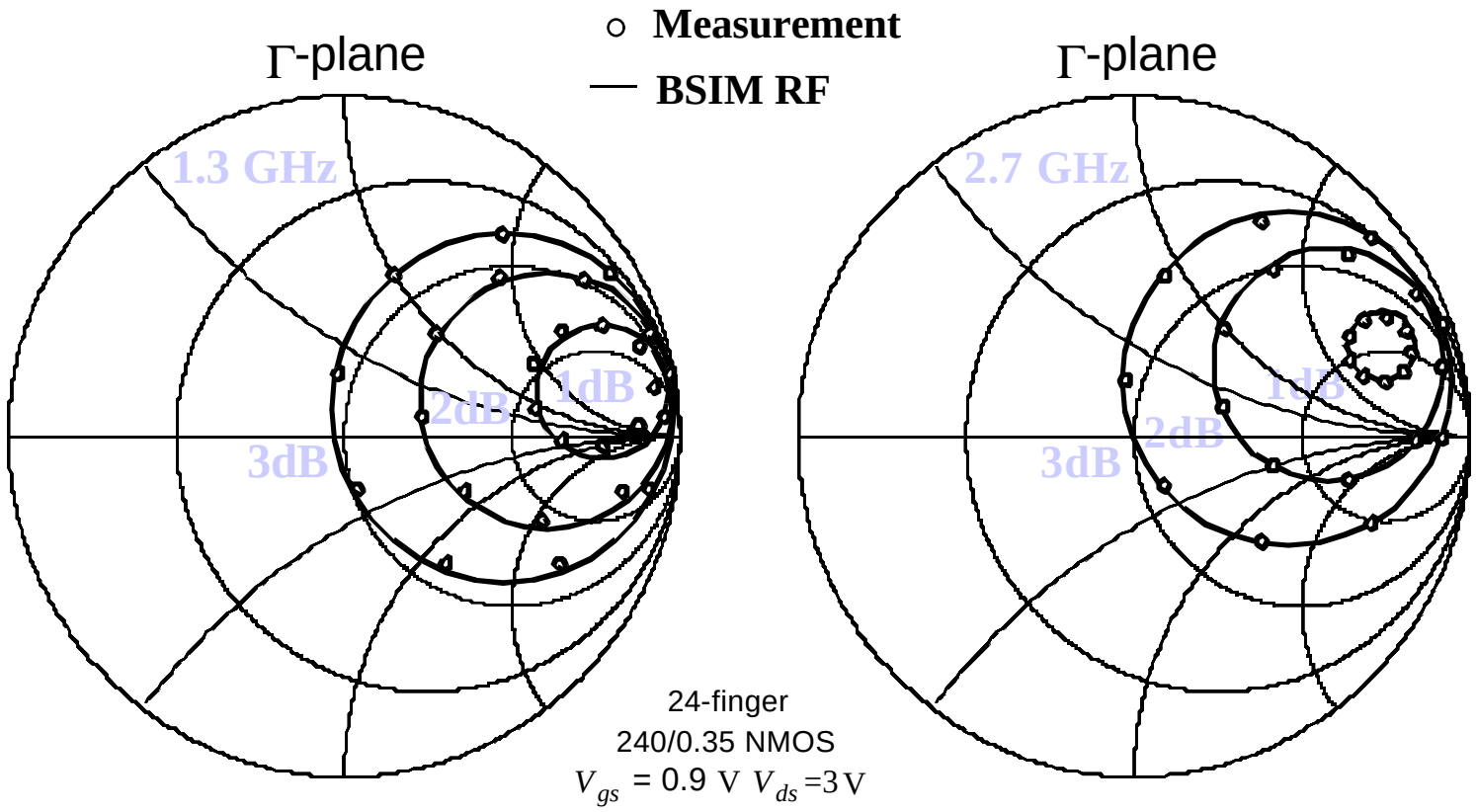
Rg = 9.5 Ω
R_{subd} = 50 Ω

24-finger
240/0.35 NMOS
V_{gs} = 0.9 V V_{ds} = 3 V

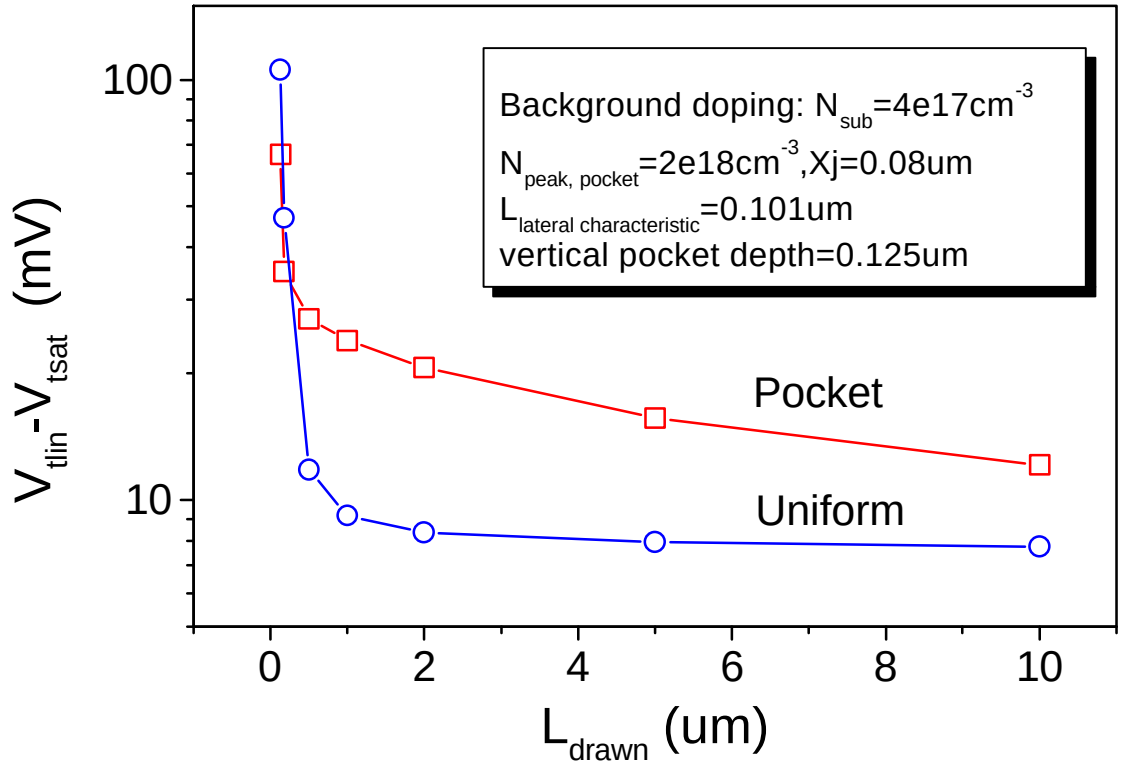




Verification With Constant Noise Contours



BSIM4 Long Channel DIBL due to Pocket Implant



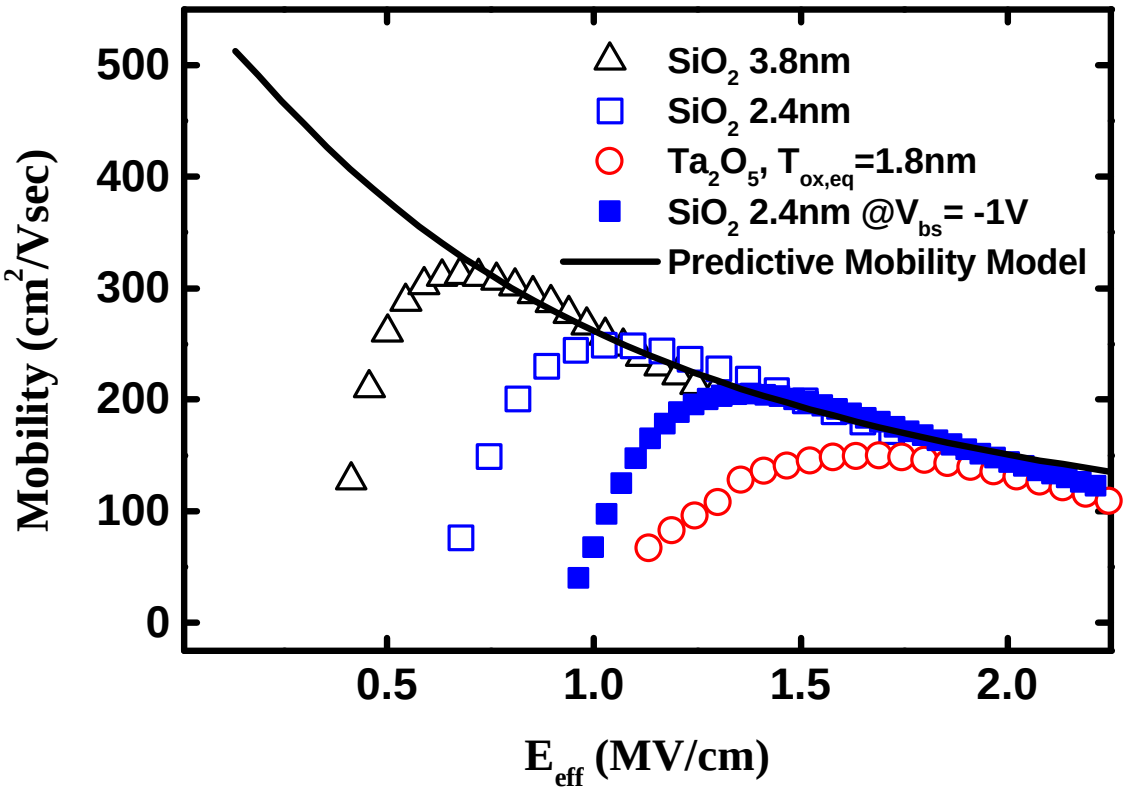
BSIM4 IV Model: *Universal Mobility*

BSIM4 retains mobMod=0 and 1 mobility models from BSIM3v3.2.2. The new mobMod=2, universal mobility model, is more accurate and suitable for predictive modeling:

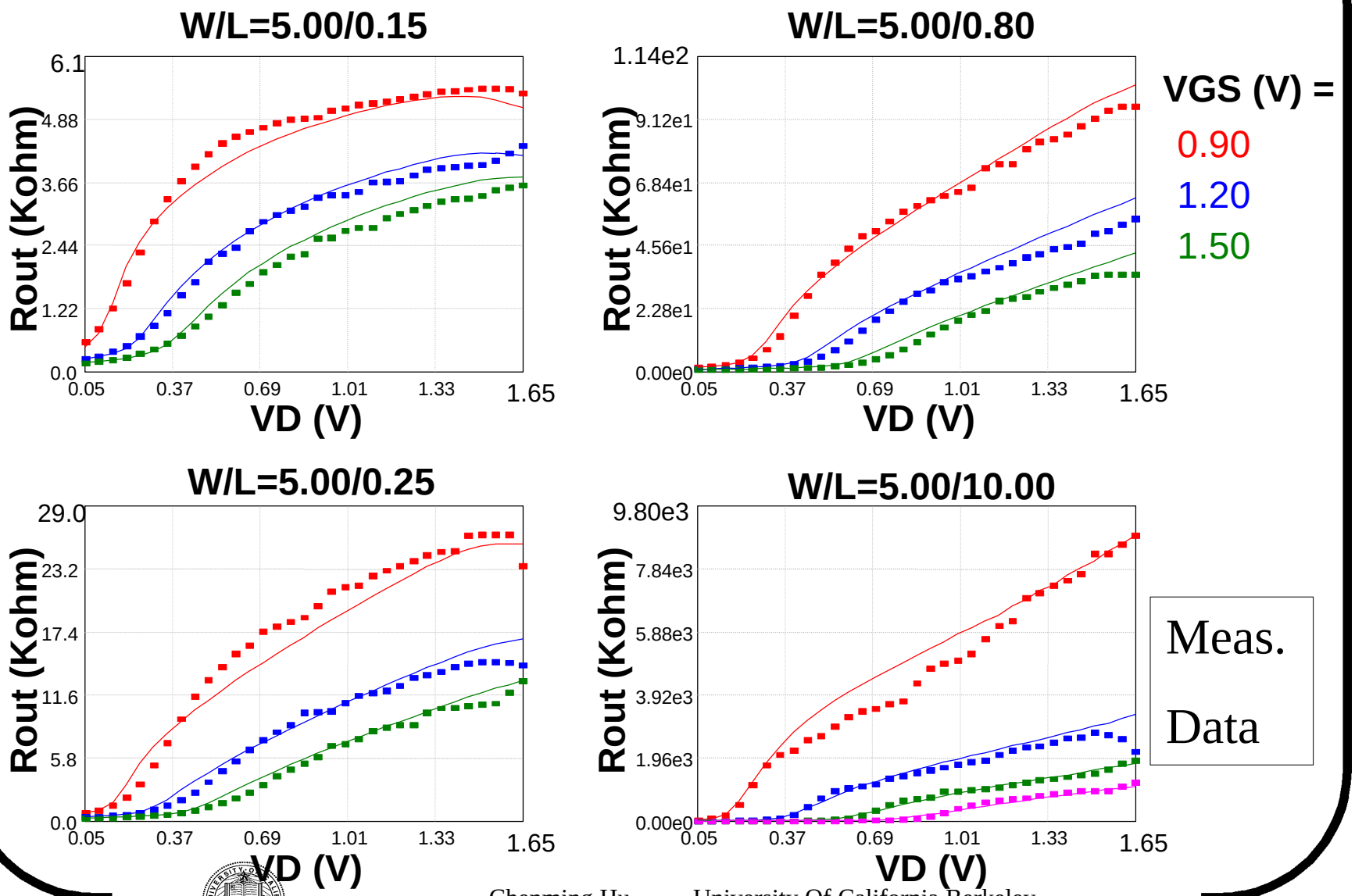
$$m_{eff} = \frac{m0}{1+\left(UA+UCV_{bseff}\right)\left[\frac{V_{gsteff}+C_0\cdot\left(Vth0-Vfb-j_s\right)}{T_{oxe}}\right]^{EU}}$$

where the constant C_0 = 2 for NMOS and 2.5 for PMOS.

Predictive Mobility Model



Verification of BSIM4 Rout Model



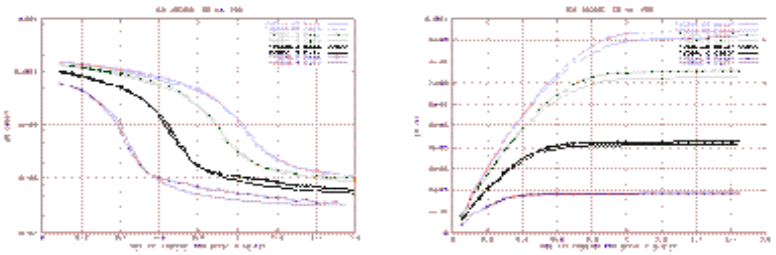
Verification of BSIM4 Rout Model

Acrobat Reader

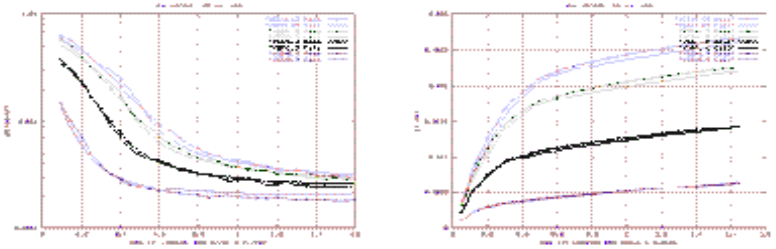
Sample IV fits: NMOS 1.5 V Process

- Much improved Gd fits
- No binning over gate length

L = 10 um



L=nominal



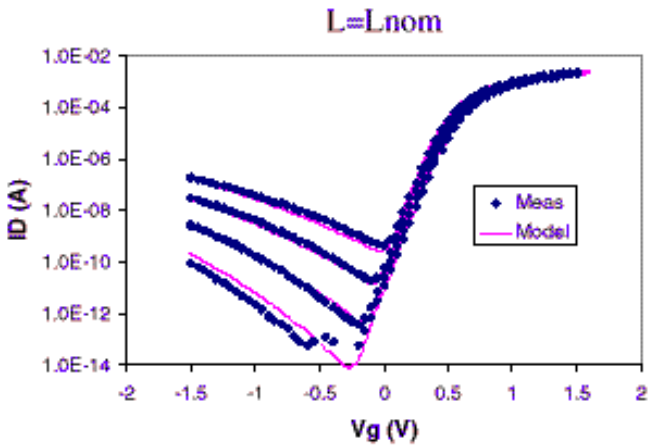
BSIM4 IV Model: *Gate-Induced Drain Leakage Current*

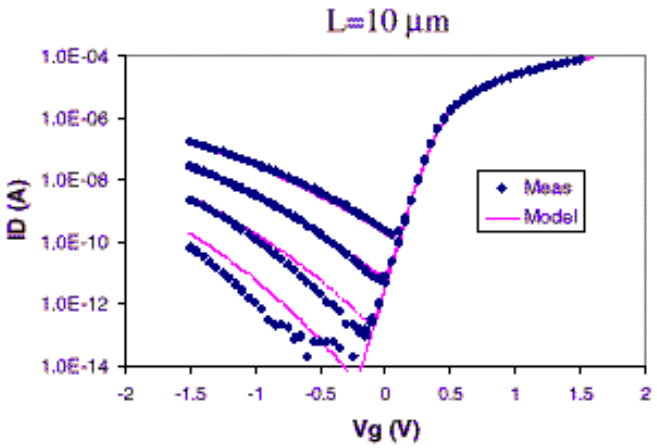
- **Verification**

Acrobat Reader

GIDL Model

- Hand fit GIDL model to one technology and one gate length
- Model scales over L using same parameter set

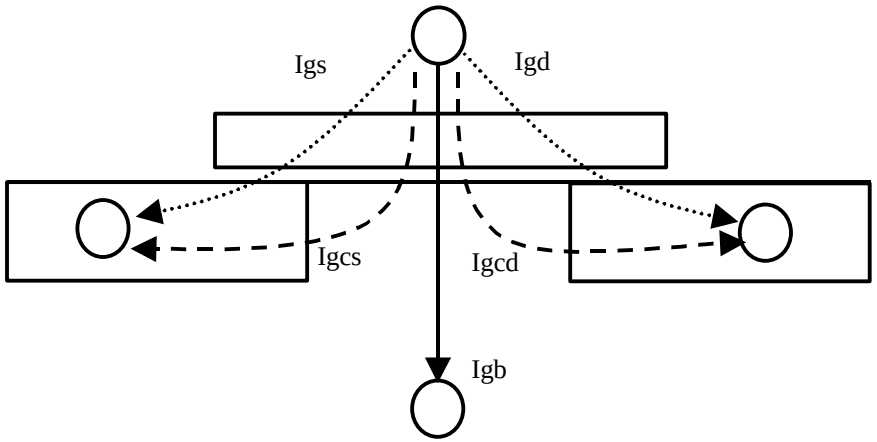




BSIM4 Gate Dielectric Tunneling Current Model

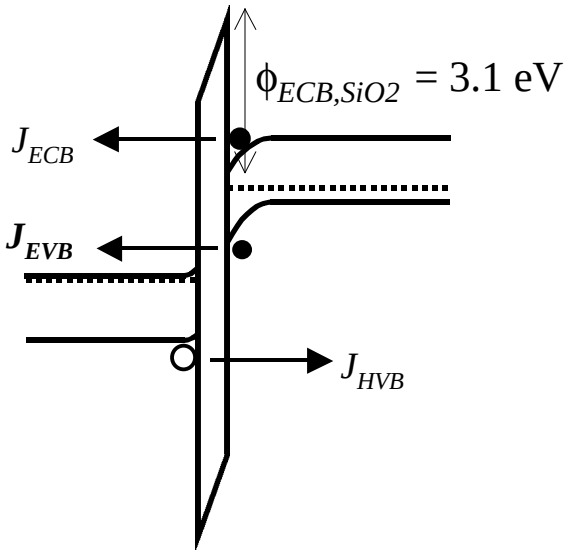
- Gate tunneling current of n^+-poly NMOS and p^+-poly PMOS are modeled, including ***Igb*** between gate and body, and ***Igc*** between gate and channel, which is partitioned between the source and drain terminals such that ***Igc = Igcs + Igcd***. Tunneling currents in the gate-source/drain overlap regions (***Igs*** and ***Igd***) are modeled as well.

- Modeled current flows for NMOST in inversion region



BSIM4 Gate Dielectric Tunneling Current Model

3. Three tunneling mechanisms are considered ECB, EVB and HVB.



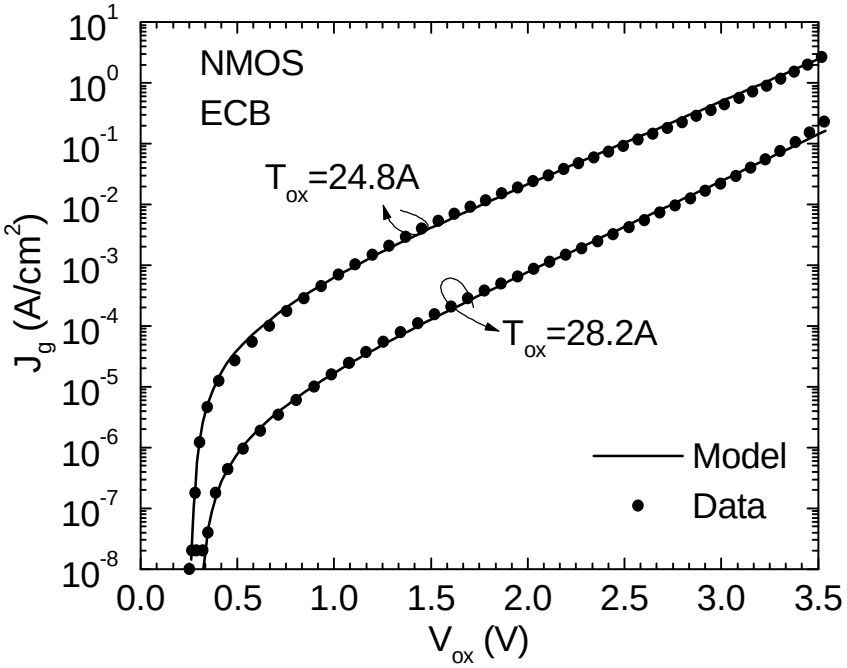
4. Equations:

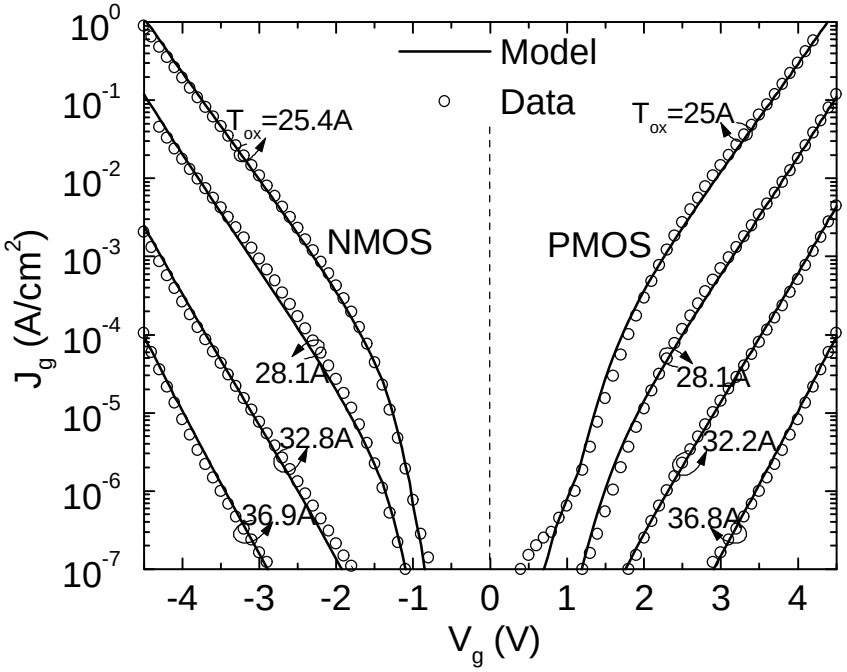
$$V_{ox} = V_{fbzb} - V_{fbeff} + k_{1ox}\sqrt{j_s} + V_{gsteff}$$

$$Igc = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gs\_eff} \cdot V_{aux} \cdot \exp\left[-B \cdot T_{oxe}\left(aigc - bigc \cdot V_{ox}\right) \cdot \left(1 + cigc \cdot V_{ox}\right)\right]$$

BSIM4 Gate Dielectric Tunneling Current Model

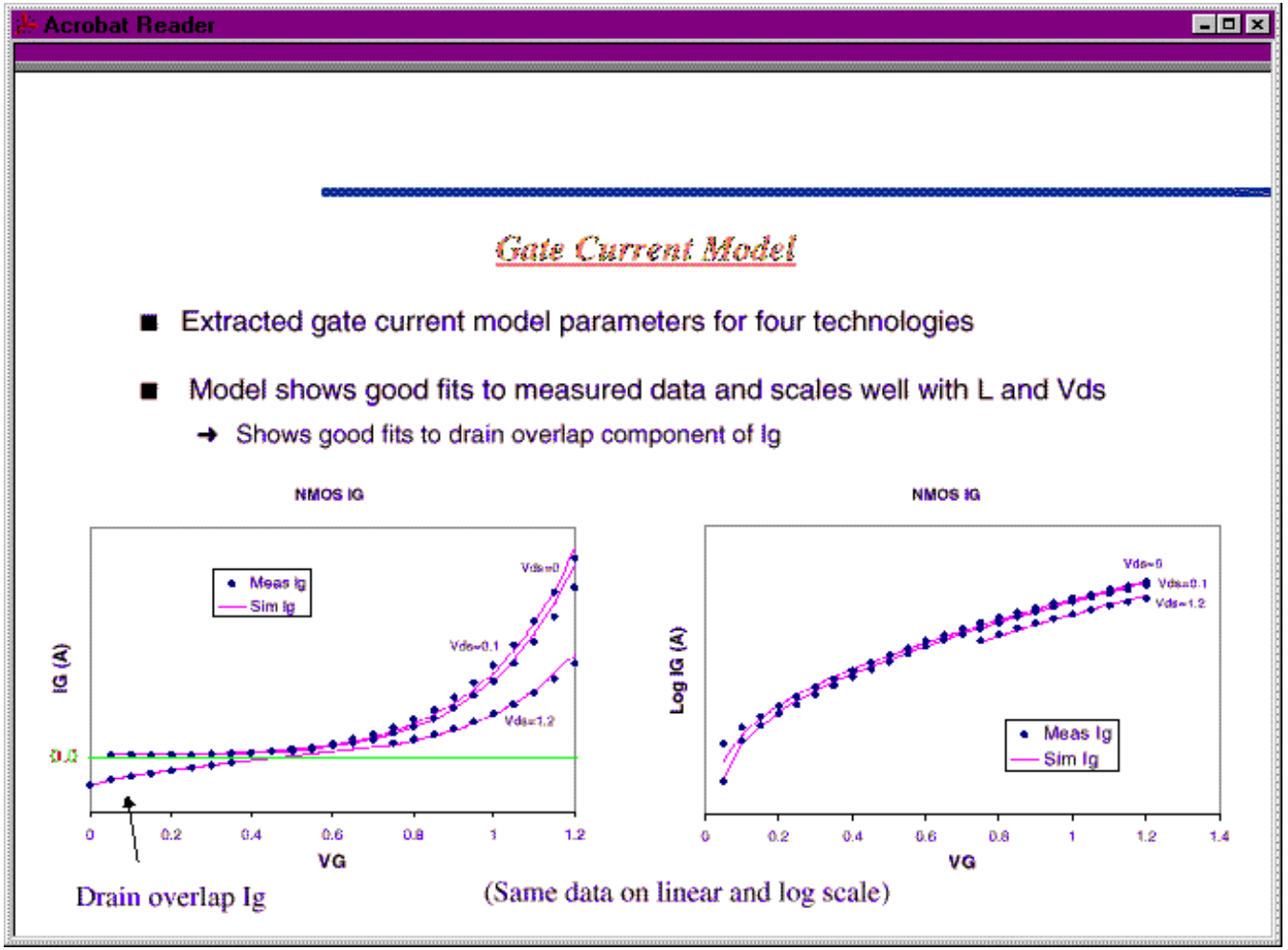
5. Verification:





BSIM4 Gate Dielectric Tunneling Current Model

5. Verification:



Gate (Equivalent) *Tox* and Dielectric Constant, and Quantum Mechanical Charge-Layer-Thickness Model

BSIM4 models charge-layer thickness (*XDC*) effect. Based on *XDC*, the effect of *Coxeff* on IV and CV is modeled.

Model parameters:

acceptance of either the electrical or physical gate oxide thickness as the model input at the user's choice in a physically accurate manner;

TOXE: Electrical gate equivalent oxide thickness;

TOXP: Physical gate equivalent oxide thickness;

TOXM: TOXE at which the other BSIM4 parameters are extracted;

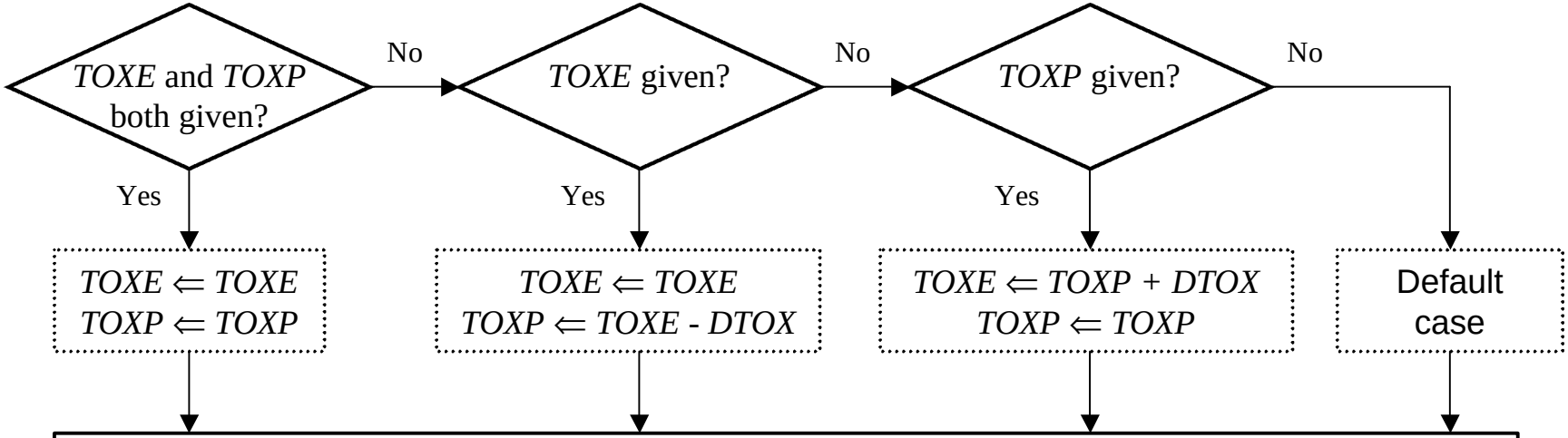
DTOX: Defined as (*TOXE* - *TOXP*).

XDC equation:

$$X_{DC} = \frac{1.9\times10^{-9}}{1+\left(\frac{V_{gsteff}+4(VTH0-VFB-\Phi_s)}{2TOXP}\right)^{0.7}}$$

Gate (Equivalent) *Tox* and Quantum-Mechanical Charge-Layer Thickness

- **Algorithm and model equations:**



- *TOXE* is used to compute: *Vth*, subthreshold swing, *Vgsteff*, *Abulk*, mobiliy, *Vdsat*, *K1OX = K1 * TOXE / TOXM*, *K2OX = K2 * TOXE / TOXM*, capMod=0 and 1, and so on; and
- *TOXP* is used to compute *Coxeff* for drain current and capMod=2 through X_{DC}.

BSIM4 Comprehensive and Versatile Layout-Dependent Parasitics Model

- Charge-Current-Capacitance (QIC) Model for series/parallel devices

Intrinsic QIC

$$QIC_{total}(Wdrawn) = QIC_{per\_finger}(Weff, Weffcv) \cdot NF$$

Overlap QC

$$QC_{total}(Wdrawn) = QC_{per\_finger}(Weffcv) \cdot NF$$

Diode IC

$$C_{jbottom,total}(Wdrawn) = A_{eff} \cdot C_{jbottom}$$

$$C_{jsw,total}(Wdrawn) = P_{eff} \cdot C_{jsw} + Weffcj \cdot C_{jswg} \cdot NF$$

$$I_{diode,sat}(Wdrawn) = A_{eff} \cdot J_{sat,bottom} + P_{eff} \cdot J_{jsw} + Weffcj \cdot J_{jswg} \cdot NF$$

BSIM4 Comprehensive and Versatile Layout-Dependent Parasitics Model

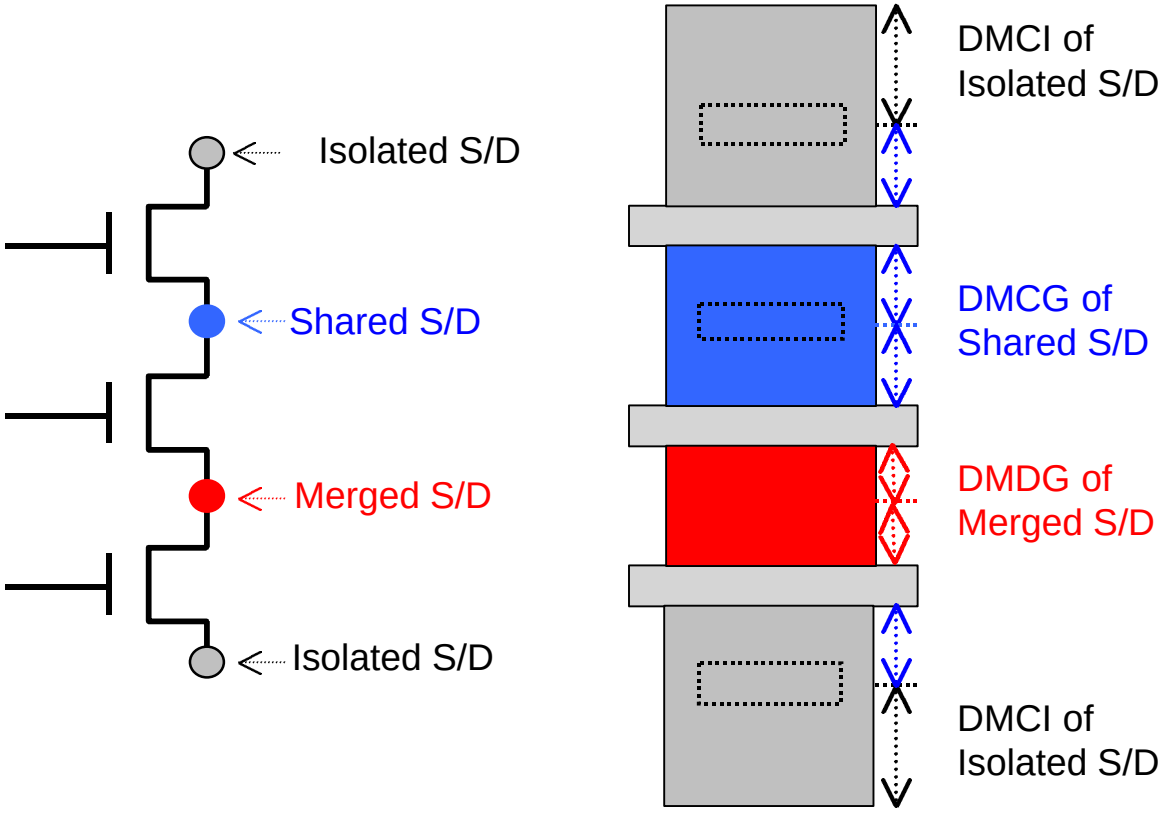
- **This model considers the effects of S/D/G and contact geometries and contact types on :**
  1. junction perimeters and areas (diode IV and CV);
  2. S/D and gate resistances;
- **This model supports multi-fingered device layout.**
- **It is able to model devices either in series, parallel or configurations.**
- **Parameters Wdrawn, Ps, Pd, As and Ad specified in the instance line are defined as the total values for a multi-finger device, not the values for each finger.**
- **Weff, per-finger device width, is defined as:**

$$Weff = \frac{Wdrawn}{NF} - 2 \cdot dW$$

- **Fourteen New parameters**.

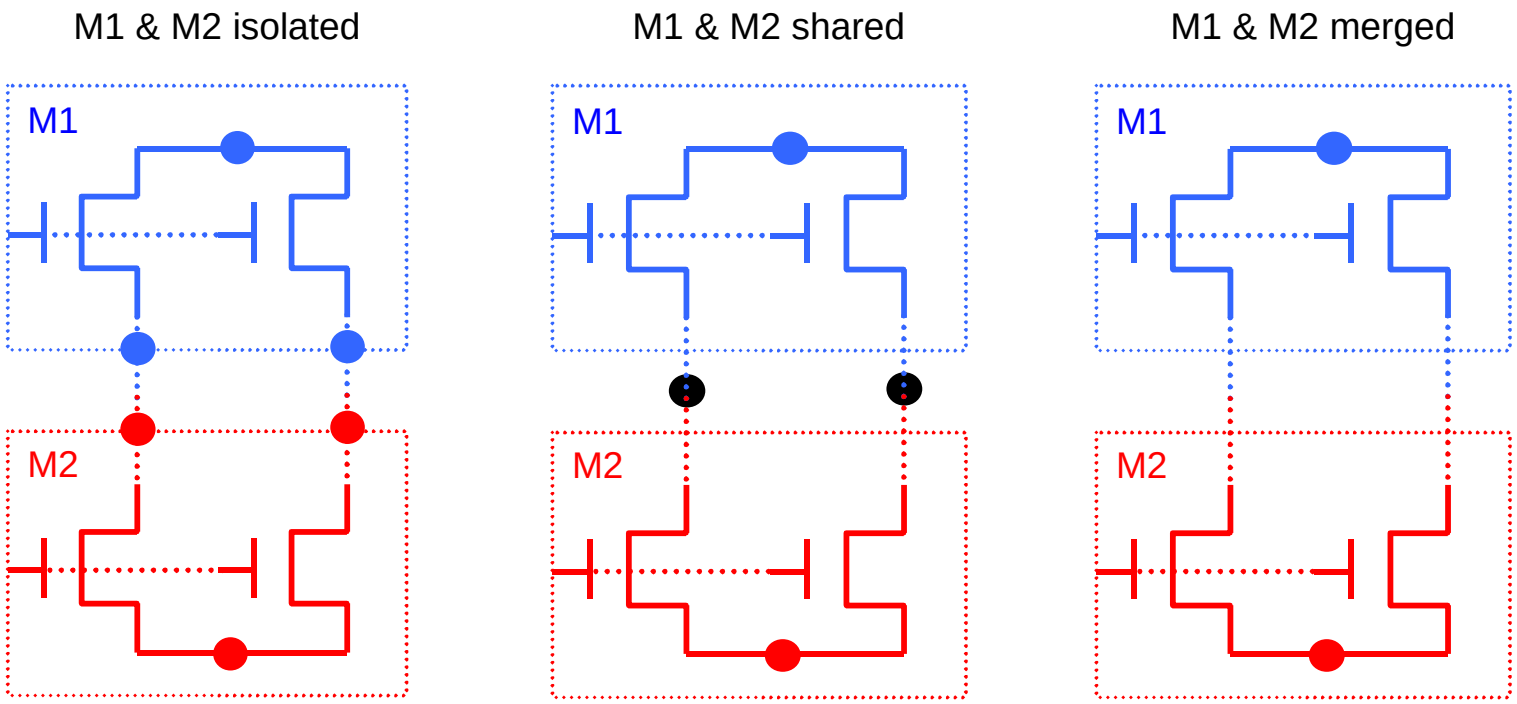
BSIM4 Comprehensive and Versatile Layout-Dependent Parasitics Model

- **Series/cascode connections: isolated, shared, and merged**



BSIM4 Comprehensive and Versatile Layout-Dependent Parasitics Model

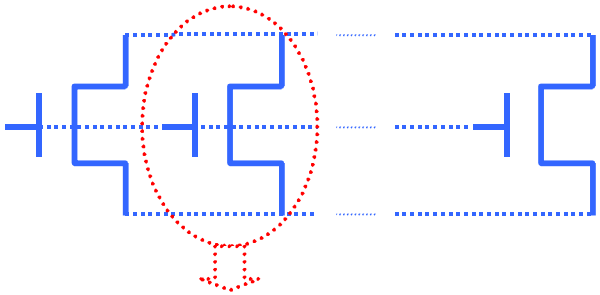
- Example: Combination of Series/Parallel Connections



BSIM4 Comprehensive and Versatile Layout-Dependent Parasitics Model

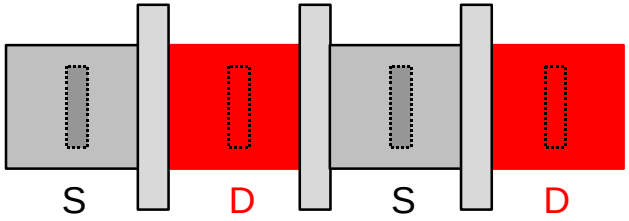
- **Multi-finger/parallel devices:**

NF (number of fingers) per-finger devices in parallel

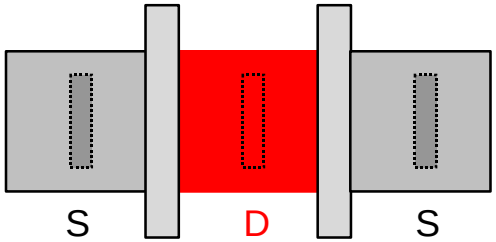


Per-finger device

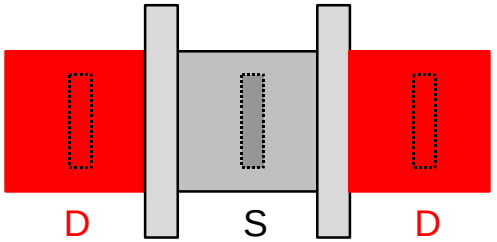
NF=Odd, MINSD is not needed



NF=Even, MINSD==0

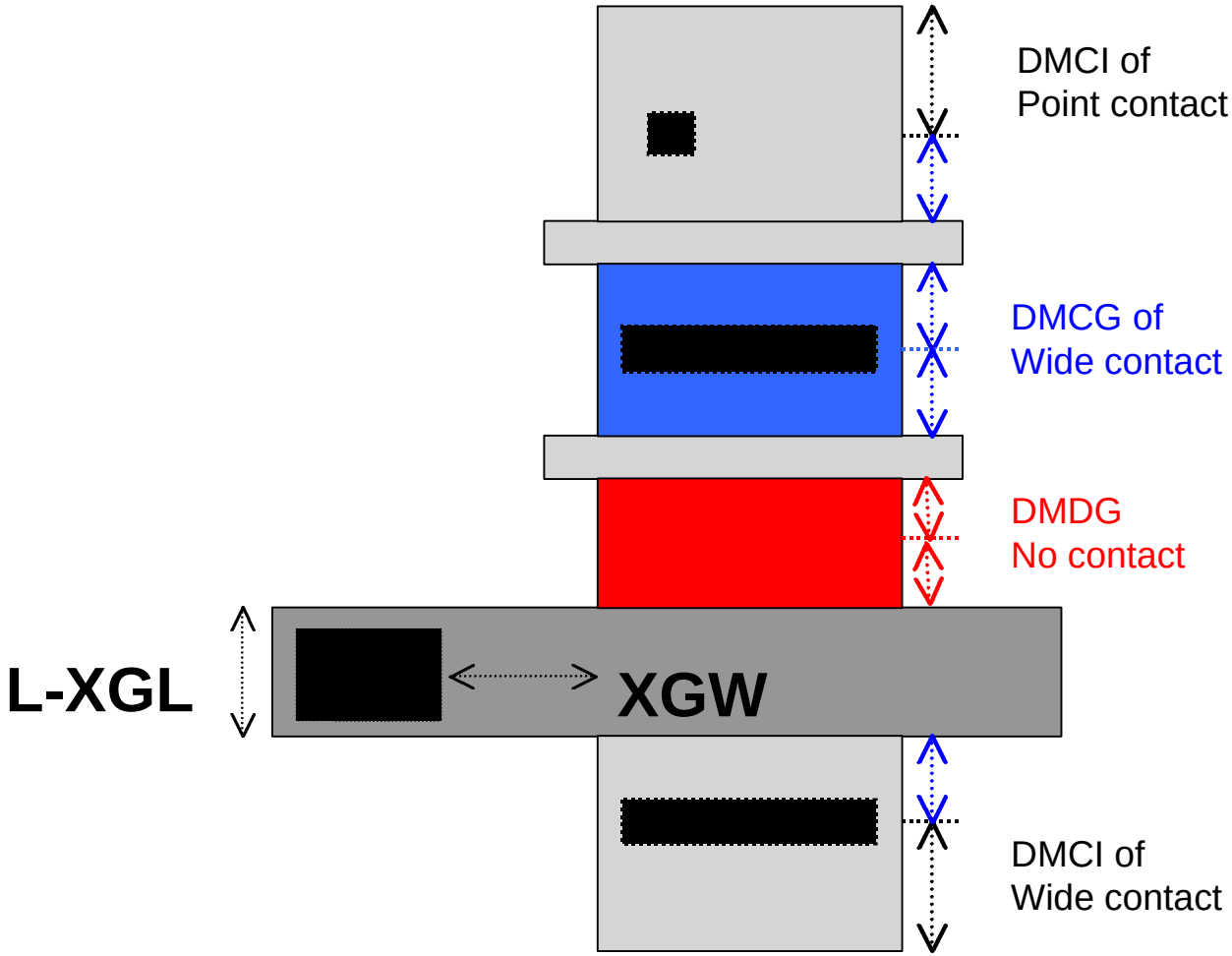


NF=Even, MINSD==1



BSIM4 Comprehensive and Versatile Layout-Dependent Parasitics Model

- S/D Diffusion and Gate Electrode Resistances



Summary

Highlights of BSIM4:

- **RF Model including the new holistic thermal noise model. Comprehensive layout-dependent parasitics model. Quantum mechanical charge thickness model in IV and CV. Gate-Induced drain leakage. Gate dielectric tunneling current, heavy pocket implant effect.**
- **Better physics should further enhance BSIM's role as a vehicle for statistical modeling and predictive modeling.**