Guest Editorial

SIGNAL integrity has become one of the most critical issues in deep submicrometer (DSM) design today. It refers to a general requirement that signals in digital and mixed-signal circuits remain within some specified margins and are tolerant to noise of any kind, so as to minimize data errors. With the continuous reduction of feature size and the consequent explosion of circuit complexity, it has become increasingly difficult to guarantee the integrity of signals. The problem is made more difficult with the advent of system-on-a-chip (SOC) design paradigms for the integration of high-speed logic and memory, significant computational power and, potentially, mixed-signal and radio-frequency circuits on the same chip.

In digital circuits, a signal integrity failure occurs when a data signal is forced to an erroneous logic state, either temporarily or permanently, causing a timing or functional error. Mechanisms such as electromagnetic coupling, capacitive crosstalk, charge-sharing, and glitches can result in logic inversion or the delay of a signal. A spurious noise signal transmitted through the substrate or the supply bus can change the electrical characteristics of devices causing similar effects, and occasionally catastrophic ones, such as dynamic latch-up.

This issue of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS includes a selection of articles derived primarily from the 1999 Custom Integrated Circuits Conference (CICC). CICC is an IEEE-sponsored international conference devoted to very large scale integrated custom integrated circuit (IC) design and related computer-aided design (CAD) techniques. The guest editors began by reviewing the 20 papers on signal integrity out of the 137 papers originally accepted for presentation at the conference. Seven of the papers solicited for submission for this special issue were accepted for publication after undergoing two cycles of review. These papers represent a good cross section of the research in this field.

In the first paper, Saleh et al. demonstrate the impact of power grid voltage (IR) drop on timing and propose a two-step relaxation-based approach to compute clock delays and skews while accounting for dynamic variations in the power supply. The approach accurately models the nonlinearity in clock trees in one simulator and analyzes the large-scale linear circuit underlying the power distribution system in a second simulator. This minimizes the CPU time for the overall analysis while providing the needed accuracy.

The topic of substrate noise modeling was the focus of three articles at CICC. Briaire and Krisch have constructed an extensive macro-model of substrate injection currents in devices using computer simulations and actual measurements. The authors have also proposed a simulator which combines switching activities and injection models to evaluate the total substrate injection spectrum. The results are useful in analyzing the potential noise injected by large digital components before they are integrated on chip.

Well noise is an issue in digital circuits due to possible dynamic latch-up. Koyama et al. develop a new technique for well noise analysis that incorporates the controllable threshold voltage scheme now used in many low-power designs. A new model for characterizing the well noise for gate array and standard cell design styles is described in this paper.

Nagata et al. describe a test chip architecture to measure substrate noise waveforms using transition controllable noise sources. A resolution of 100 ps and 100 μV is achieved in the substrate noise measurements using indirect sensing techniques and direct probing.

Three articles present signal integrity aware techniques for physical design and optimization of IC’s. Visweswariah et al. describe a methodology to optimize digital circuits in the presence of noise due to charge-sharing and glitches. The optimization problem is formulated as a set of equality constraints derived from semi-infinite noise constraints, and is applied to the transistor sizing problem in dynamic circuits.

The technique proposed by Liu et al. improves upon an existing detailed routing method by spacing the interconnect to meet a set of constraints on the maximum attainable crosstalk. The algorithm perturbs a wire over a set of subintervals, selected so as to show monotonic or unimodal crosstalk variation, thus avoiding the need of solving a series of nonlinear optimization problems. The method is gridless and is not restricted by a particular interference model.

Phelps et al. propose a novel numerical search algorithm for circuit optimization. The highlights of the algorithm include population-of-solutions principles, introduced by evolutionary algorithms, and a new pattern search scheme. The main advantage of the method is its search robustness and efficiency, which allows one not to give up the accuracy of a full-blown simulator. Another major advantage is the suitability of the algorithm to parallelism, thus ensuring a even higher synthesis speed.

EDOARDO CHARBON, Guest Editor
Cadence Design Systems, Inc.
San Jose, CA 95134 USA

RESVE SALEH, Guest Editor
Simplex Solutions, Inc.
Sunnyvale, CA 94086 USA
Edoardo Charbon (S’90–M’92) received the M.S. degree in electrical and computer engineering (communication theory) from the University of California, San Diego, and the Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley, in 1995 and 1991, respectively. He received the Diploma in electrical engineering from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, in 1988.

Between 1989 and 1993, he was an Academic Visiting Fellow with the University of Waterloo, Waterloo, ON, Canada, and the research laboratories of Texas Instruments, Dallas, and Hewlett-Packard, Santa Rosa, CA. In 1995, he joined Cadence Design Systems, Inc., San Jose, CA, where he worked on advanced acceleration techniques for physical design synthesis applications. Since 1998, he has been the architect of Cadence’s company-wide initiative on intellectual property protection. His research interests include CAD for radio-frequency integrated circuits, methodologies for intellectual property protection, substrate modeling and characterization, superconducting parasitic analysis, and micromachined sensor design. He has published over 40 articles in technical journals and conference proceedings, and two books on mixed-signal computer-aided design and substrate noise.

Dr. Charbon is a member of a Swiss National Science Foundation fellow. He is currently serving on the technical committees of the Custom Integrated Circuits Conference and the VSI Alliance. For his work, he has received a product quality award and several inventor recognitions, and was recently granted a patent for sequential circuit watermarking techniques.

Resve Saleh (S’78–M’79) received the B.S. degree in electrical engineering from Carleton University, Ottawa, ON, Canada, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of California, Berkeley.

In 1995, he co-founded Simplex Solutions, Inc., Sunnyvale, CA, to address deep submicrometer-integrated circuit verification and currently serves as Chairman. Prior to starting Simplex, he spent ten years as a Professor in the Department of Electrical and Computer Engineering and the Department of Computer Science at the University of Illinois, Urbana. He has also worked for Toshiba Corporation in Japan, Tektronix in Beaverton, OR, and Mitel Corporation in Ottawa, Canada. He began his career as a Software Engineer with Bell-Northern Research in Ottawa, Canada. He was granted a patent for nonlinear frequency domain analysis in 1997. He has written two books on analog and mixed-mode simulation and published over 50 conference papers and journal articles.

Dr. Saleh has served as technical program chair, conference chair, and general chair for the Custom Integrated Circuits Conference in 1993, 1994, and 1995, respectively. He has served on the technical program committees of the Design Automation Conference, International Conference on Computer Design, and, most recently, the International Symposium on Quality in Electronic Design. From 1992-1995, he held the position of chairman of the IEEE Standards Coordinating Committee 30 on Analog Hardware Description Languages (AHDL). He also received an inventor recognition award from the Semiconductor Research Corporation in 1991. He is currently an Associate Editor for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS. He received a Presidential Young Investigator Award in 1990 from the National Science Foundation.